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PtGe-Source/Drain Ge p-MOSFET with High On/Off Ratio and Low Parasitic Resistance

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Abstract

We investigated fabrication of PtGe/Ge contacts with low hole barrier height (Φ_{BP}) and its electrical passivation. A PtGe/n-Ge contact passivated by an ultrathin SiO_2/GeO_2 bilayer showed high electron barrier height (Φ_{BN}) of 0.64 eV, indicating Φ_{BP}~0 eV and an on/off ratio of ~10^6. The p-MOSFET with an equivalent oxide thickness (EOT) of 3.4 nm was fabricated using PtGe contacts as metal source/drain(S/D), which showed well-behaved transistor operation. From the investigation of device performance, we showed that the on/off ratio of drain current and the parasitic resistance of PtGe-S/D were much superior compared with those of HfGe-S/D p-MOSFET.

1. Introduction

Ge is of great interest as a high mobility channel material for future CMOS devices because of its high intrinsic carrier mobility. However, it is difficult to form shallow source/drain (S/D) junctions with low sheet and contact resistances because of the low dopant solubility. Metal S/D MOSFETs are a promising solution to these problems.[1,2)] To realize high performance, metal/Ge contacts with low hole barrier height (Φ_{BP}) and low electron barrier height (Φ_{BN}) are needed for p- and n-MOSFETs, respectively. In this study, we focussed on the fabrication of a contact with low Φ_{BP}.

Another important issue for fabrication of metal/Ge contacts is the surface passivation. A surface layer on a bared n-Ge substrate is usually depleted owing to Fermi-level-pinning (FLP).[3,4)] Thus, good rectified characteristics can be simply obtained. However, the peripheral surface-state generation current (I_p) increases when the surface passivation is inadequate. Since the surface passivation is essential for the device, the passivation technique is also as important as a selection of low-Φ_{BP} material.

In this paper, we report electrical properties of a PtGe/Ge contact passivated by an ultrathin SiO_2/GeO_2 bilayer. We also report the fabrication and performance of p-MOSFETs featuring PtGe-S/D, which had a gate stack structure of $TiN/Al_2O_3/SiO_2/GeO_2$/Ge and an EOT of 3.4 nm.

2. Fabrications of PtGe/Ge Contact and p-MOSFET

The substrates used were n-type (100) Ge with a resistibity of 0.4 Ω·cm, corresponding to an donor concentration of 5×10^{15} cm^{-3}.The chips were dipped in dilute HF solution followed by rinsing in DI water. After that, Pt and Ti were deposited by rf sputtering. Note that the Ti film played a role of a cap for a Pt film because the Pt film without the Ti cap was partially peeled by DI water rinsing. Ti/Pt/Ge contacts with an area of 180×400 μm^2 were formed by lift-off process. Then, the Ti/Pt/Ge contacts were followed by PMA at a temperature in the range of 400-500°C for 30 min in N_2. The PtGe/Ge contact was passivated using the following two methods after 0.5 % dilute HF cleaning and DI water rinsing. The first method was bilayer passivation (BLP), by which a Ge surface was electrically passivated by an ultrathin SiO_2/GeO_2 bilayer. The second method was electron cyclotron resonance (ECR) plasma deposition.[5)] The substrate temperature in BLP and ECR plasma deposition was 350°C and 130°C, respectively. Then, the samples were cooled down to RT, and a 50 nm-thick SiO_2 films were deposited. PDA was performed at a temperature in the range of 400-500°C for 30 min in N_2. After the passivation, contact holes were opened, and Al electrodes were formed by lift-off techniques. Finally, contact annealing was carried out at 300°C for 10 min in N_2.

Figure 1 illustrates our gate-last process for the metal S/D p-MOSFET. After the BLP, an Al_2O_3 film with a thickness of 4.0 nm was deposited by ALD at 300°C. Al/TiN films were deposited and fabricated as metal gate.

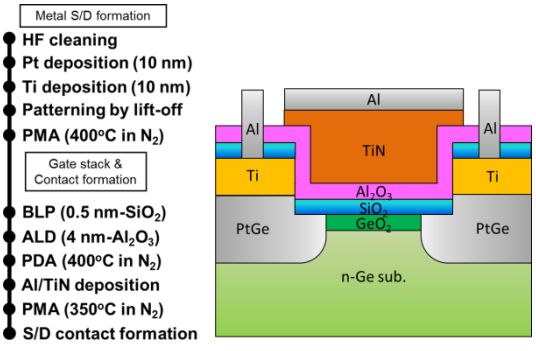

Fig. 1 Fabrication process for the PtGe-S/D p-MOSFET.

3.Results and discussion

The Φ_{BN} and the ideality factor (n) were obtained from the forward *I-V* characteristics. Figures 2(a) and 2(b) show the vertical and lateral *I-V* characteristics of a PtGe/Ge contact without surface passivation and the contacts with BLP and ECR plasma deposition, respectively,

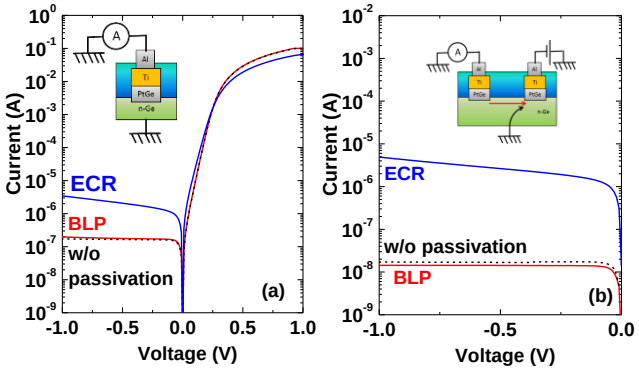

Fig. 2 (a) Vertical and (b) lateral *I-V* characteristics of a PtGe/Ge contact without surface passivation and the contacts with BLP and ECR plasma deposition.

where PMA and PDA temperature were 500 and 400°C, respectively.

A contact without surface passivation shows excellent rectifying characteristics with a Φ_{BN} of 0.64 eV and n of 1.02. A contact with BLP was similar to a contact without surface passivation and showed a lower leakage-current, a high on/off ratio of ~10^6, a Φ_{BN} of 0.64 eV, and an n of 1.02. On the other hand, the properties passivated by ECR plasma deposition method were much worse than that of BLP despite the use of SiO_2/GeO_2 passivation. Therefore, the excellent characteristics of a contact with BLP are attributable to good passivation effect by the present BLP method on a Ge surface. Thus, we concluded that a PtGe contact with BLP is useful as S/D in Ge p-MOSFET and the performance is maintained for PMA and PDA in the range of 400-500°C.

Figure 3 shows the drain current (I_D) and source current (I_S) vs drain voltage (V_D) characteristics for the fabricated p-MOSFET. Here, the flat band voltage (V_{FB}), the threshold voltage (V_{TH}), and EOT were +0.08 V, -0.30 V, and 3.4 nm, respectively; channel length (L) and width (W) were 100 and 390 μm, respectively. The channel conduction is well controlled by the gate voltage (V_G), implying that the PtGe contact with BLP works well as S/D. Furthermore, the difference between I_D and I_S is relatively small, implying that substrate current (I_{SUB}) is considerably small thanks to high Φ_{BN} of the PtGe/Ge drain-contact.

Figure 4 shows I_D, I_S, and I_{SUB} vs V_G characteristics with V_D= -0.01, -0.1, and -1 V. On/Off ratios of I_D at V_D of -0.1 V and -1 V were 6.2×10^2 and 7.2×10^2, respectively, which are almost 10 times larger than that of HfGe-S/D MOSFET with an EOT of 3.2 nm.[6] The subthreshold slopes (SS) of I_S at V_D=-0.01 V was 85 mV/dec, corresponding to $D_{it}=2.3\times10^{12}cm^{-2}eV^{-1}$. Figure 5 shows the field-effect hole mobility (μ_h). The μ_h was evaluated using the data from V_D=-0.01 V with the relation $\mu_h=g_m/[(W/L)C_{ox}V_D]$, where g_m is the transconductance and C_{ox} is the inversion channel capacitance. These three plots accord with each other and show peak μ_h of ~200 cm^2/Vs. For comparison, the results obtained from HfGe-S/D p-MOSFETs are also shown in Fig. 5.[6] It is clear that μ_h deteriorated with a decrease in L and with a negative increase in V_G. The parasitic resistances for PtGe- and HfGe-S/D were estimated as ~50 and ~300 Ω, respectively. Thus, we concluded a PtGe contact with BLP is very useful as S/D in Ge p-MOSFET

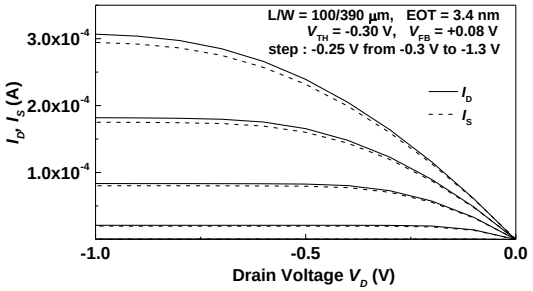

Fig. 3 I_D and I_S vs V_D characteristics of PtGe-S/D p-MOSFET.

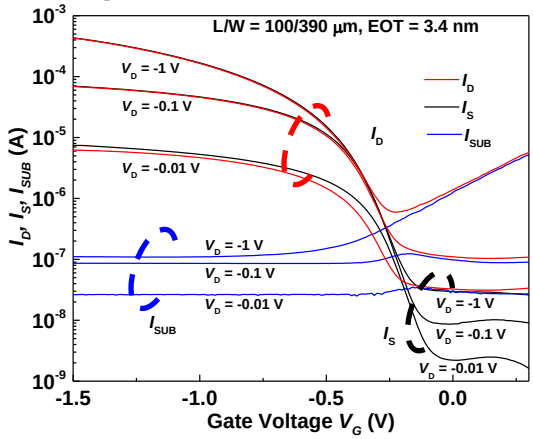

Fig. 4 I_D, I_S and I_{SUB} vs V_G characteristics with V_D=-0.01, -0.1 and -1 V.

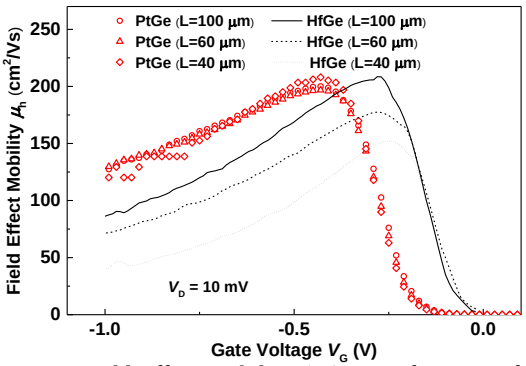

Fig. 5 Field effect mobility (μ_h) as a function of V_G for p-MOSFETs.

4. Conclusions

We established a method for fabrication of a PtGe/Ge contact with low Φ_{BP} and its electrical passivation. The PtGe/Ge contacts with BLP showed Φ_{BP} of ~0 eV and high on/off ratio of ~10^6. The p-MOSFET with an EOT of 3.4 nm was fabricated using the PtGe-S/D and demonstrated their operation. The transfer characteristics of I_D indicated an on/off ratio of ~10^3, which was one order of magnitude higher than that of HfGe-S/D p-MOSFET. The parasitic resistance could be decreased down to 1/6 using PtGe-S/D instead of HfGe-S/D.

5.References

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