

Formation of Single Crystalline Silicon with Midair Cavity for Meniscus Force-Mediated Local Layer Transfer and Fabrication of High-Performance MOSFETs on Insulator

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Abstract

We attempted to control size and shape of the SiO_2 column supporting the SOI layer by implantation for improvement of transfer yield. The column size was controlled by etching time and the minimum size was 104 nm. In case of implanted samples, the transfer yield of SOI layers was significantly improved to 95% under a condition of P^+ dose of $1 \times 10^{15} \text{ cm}^{-2}$ by optimizing the column size and shape. N-channel MOSFETs fabricated using the films on insulator at 300°C showed a field-effect mobility of $505 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ on average.

1. Introduction

Si CMOS technology is approaching the end of scaling due to unavoidable physical limitations. Therefore, three-dimensional (3D) integration technology [1] is studied intensively. In 3D integration technology, through-silicon via (TSV) is an essential process in front end of line (FEOL) and back end of line (BEOL). In case of TSV in FEOL, the poly-Si is used as a wiring material to endure high process temperature ($> 600^\circ\text{C}$). However, the resistivity of poly-Si is 2 or 3 orders of magnitude larger than that of metal. If there is a formation technology that single crystalline Si layers are stacked on an insulator at a low temperature, a metal is used as all the electrical wiring.

In our previous work, we have reported transfer of Si films with midair cavity to a counter substrate at a low temperature by using meniscus force-mediated layer transfer (MLT) technique [2]. In addition, we have demonstrated that silicon-on-insulator (SOI) on midair cavity was oxidized for formation of good MOS interface [3]. However, there is a critical issue of the MLT technique, that is low transfer yield of $\sim 20\%$. Figure 1 shows process steps to

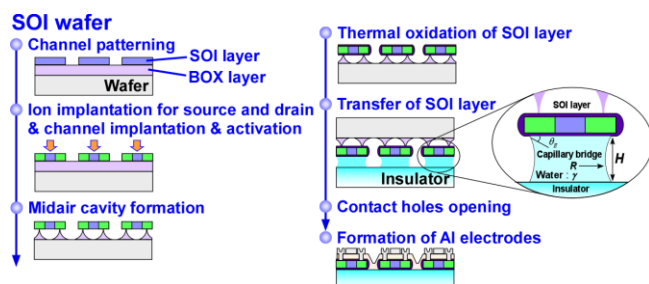


Fig. 1 Schematic diagram of a process flow of the Si MOSFET fabrication on insulator by MLT technique.

apply MLT technique to MOSFET fabrication on insulator. In Fig. 1, we consider that the SiO_2 column size and shape in midair cavity affects MLT yield. In order to control the column size and shape, we focus on ion implantation of the SOI wafer.

In this work, we observe SOI layers with midair cavity after ion implantation and thermal oxidation, and attempt to improve transfer of the SOI layers to insulating substrate. Moreover, MOSFETs using the films are fabricated.

2. Experimental

The thicknesses of SOI layer (p-Si (100)) and BOX layer are 80 and 400 nm, respectively. An SOI layer is patterned to a device shape by photolithography and chemical dry etching as shown in Fig. 2. Next, Phosphorus ions (P^+) were implanted into source and drain regions of a part of samples with a 7° tilt angle in the dose range from 1×10^{14} to $2 \times 10^{15} \text{ cm}^{-2}$ at 40 keV. Here, the ion acceleration voltage was determined to set the projection range to a position near SOI/BOX interface for formation of good contact between the transferred SOI layer and metal electrodes. And the implanted samples were annealed at 1000°C for the activation of impurities. Then the BOX layer is etched by 25% HF solution at 30°C to form midair cavity. The size of residual SiO_2 columns was controlled by etching time. Thermal oxidation of SOI layers with midair cavity was performed in dry oxygen at 1000°C for 4 min. After that, the SOI layer was transferred to an insulator by MLT technique. In this work, glass (Coring Eagle 2000) is used as an insulating substrate. The samples were heated at 80°C on a hot plate for 15 min for layer transfer.

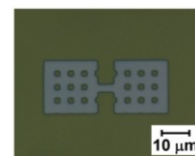


Fig. 2 Optical microscope images of top view of device pattern formed on SOI layer.

3. Results and discussion

Figures 3 show SEM images of side view of SiO_2 column of the samples without and with ion implantation (I/I). Here, the column size (S) is defined by the narrowest width of the column. The size of the samples without I/I was decreased by increasing etching time and it was confirmed that minimum of column size was 137 nm after 390 s etching. On the other hand, the column shape of the implanted samples changed to tapered side wall. As a result, the SiO_2 column near SOI layer was narrow and the size was 104 nm after

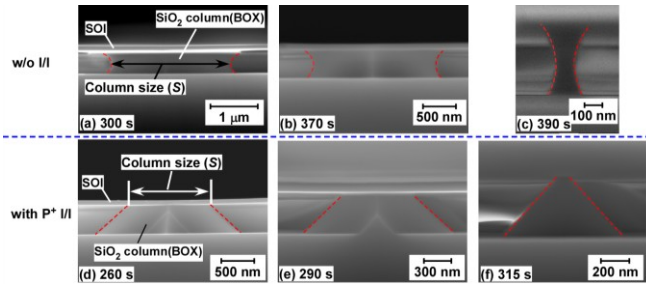


Fig. 3 SEM images and schematic diagrams of side view of SOI layer with midair cavity (a) ~ (c) without I/I and (d) ~ (f) with I/I at each etching time.

315 s etching. We consider that the taper shape of the BOX layer with I/I was formed because of the difference of the etching rate depending on P^+ concentration toward the BOX depth direction. Detailed etching simulation has been performed and the tapered shape was well reproduced [4]. This result indicates setting the projection range of I/I near the SOI/BOX interface, the shape of the SiO_2 column can be well controlled. Next, transfer of the SOI layers to insulator was performed. Transfer yield as a function of column size is plotted in Fig. 4. Here, the transfer yield is defined as the number of transferred SOI patterns to insulator divided by the total number of initial pattern on SOI wafer. In case of as-prepared and oxidized SOI layers without I/I as shown in Fig. 4 open circles and open squares, the transfer yield was low (the maximum yield of 35%). For the samples implanted with doses of 1×10^{14} and $1 \times 10^{15} \text{ cm}^{-2}$, the transfer yield was significantly improved to 95% as shown in Figs. 4 and 5. In contrast, the SOI layers implanted with a dose of $2 \times 10^{15} \text{ cm}^{-2}$ were not transferred at all. The large bend of the implanted SOI layer with midair cavity after oxidation was observed (the height difference of the layer of $\sim 300 \text{ nm}$). The layers were not transferred to an insulating substrate because the long distance between the SOI layer and insulator generated less meniscus force. These results indicate that the optimum condition of implantation dose is $1 \times 10^{15} \text{ cm}^{-2}$ in order to transfer the SOI layer to insulator.

Finally, the n-channel MOSFETs using the films were fabricated. The P^+ implantation for source/drain regions was performed by utilizing the optimum condition (dose: $1 \times 10^{15} \text{ cm}^{-2}$, acceleration energy: 40 keV). The BF_2 ions for channel doping were implanted at a dose of $2 \times 10^{11} \text{ cm}^{-2}$ and acceleration energy of 30 keV. And, the sample is

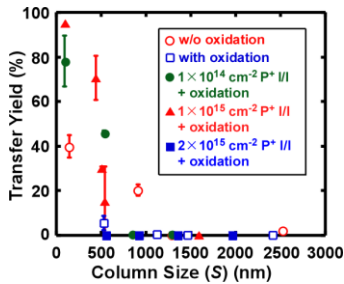


Fig. 4 Transfer yield plotted with respect to column size S .

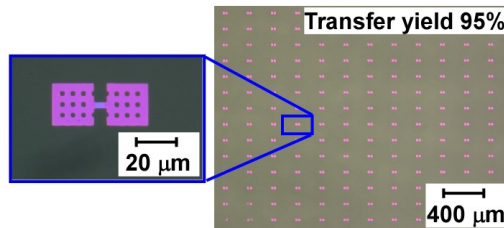


Fig. 5 Optical microscope images of oxidized SOI layers implanted with a dose of $1 \times 10^{15} \text{ cm}^{-2}$ transferred to insulator.

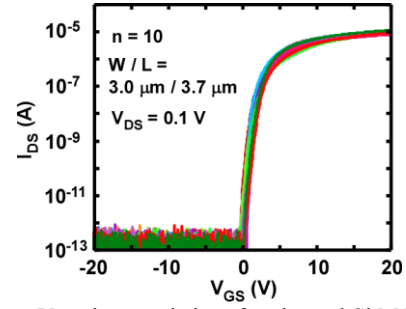


Fig. 6 $I_{DS} - V_{GS}$ characteristics of n-channel Si MOSFETs on insulator.

heated at 1000°C for the activation of impurity and oxidation. Thickness of oxidation is 6 nm. After transfer of the SOI layer, additional 193-nm-thick gate SiO_2 was deposited by PECVD. Then contact holes were opened. After formation of Al electrodes, PMA was performed at 300°C . The transistors were fabricated at maximum temperature of 300°C after transfer. From transfer characteristics of ten MOSFETs as shown in Fig.6, the average values and standard deviations ($\pm \sigma$) were field-effect mobility (μ_{FE}) of $505 \pm 76 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, threshold voltage (V_{th}) of $2.47 \pm 0.67 \text{ V}$ and S factor of $324 \pm 54 \text{ mV/dec}$, respectively. We demonstrated that fabrication of n-channel MOSFETs with uniform characteristics on an insulator substrate by MLT technique.

4. Conclusions

The SiO_2 column size was controlled by etching time and the minimum of column size was 137 nm. And, the shape of the column was controlled by implantation. The transfer yield was improved by decreasing the column size, and the maximum of the transfer yield was 95% in case of an implantation dose of $1 \times 10^{15} \text{ cm}^{-2}$. The MOSFETs fabricated using the transferred Si films at maximum process temperature of 300°C showed μ_{FE} of $505 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, V_{th} of 2.47 V and S factor of 324 mV/dec. on average. These results suggest that the MLT technique is very promising to apply to MOSFET fabrication process on an insulator for 3D layer stacking.

Acknowledgements

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