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Comprehensive characterization of generated trap sites in gate insulator using advanced stress-induced leakage current simulator

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Abstract

The noise simulator that we had developed was extended to stress-induced leakage current (SILC). It showed good agreement with the measurement results and obtained trap site density for each stress condition. In addition, SILC variability simulation was performed, and we found that one-step trap-assisted tunneling cannot explain the anomalous large SILC, but two-step trap-assisted tunneling can explain it.

1. Introduction

The reliability of a gate dielectric, such as time-dependent dielectric breakdown (TDDB), negative bias temperature instability (NBTI) and stress-induced leakage current (SILC), has been a critical issue in the scaling of transistors. In recent years, many experimental results for random telegraph noise (RTN) have been reported [1]. Inatsuka et al. reported that SILC has large variability for small devices, called anomalous SILC, and also shows RTN [2]. We reported the simulation model of RTN, and it showed good agreement with experimental results for the amplitude and time constants of trapping and de-trapping[3-5]. In this paper, we report the extended RTN simulator and its use to calculate SILC, and show the characteristics of generated trap sites by fitting the measurement results. In addition, the variability of SILC is estimated by using the developed SILC simulator.

2. Comparison of simulation and measurement

The RTN simulation and SILC simulation model is shown schematically in Fig.1. Discretized traps are arranged randomly in the real and energy spaces [3, 4]. Trapping and de-trapping processes are made to occur by using a Monte Carlo method based on the capture time constant τ_c and emission time constant τ_e of each trap. We consider energy transitions based on the multiphonon-assisted model [5,6]. The model proposed by Herrmann and Schenk [6] reproduces only trapping from the Si substrate and de-trapping to the poly-Si gate in order to calculate the trap-assisted tunneling current. For RTN simulation, we extended the model to reproduce the behavior of de-trapping to the Si substrate and trapping from the poly-Si gate [5]. Therefore, we can simulate the SILC and RTN with the same model.

Figure 2 shows the J_g vs. V_g curves for T_{ox}=6nm and T_{ox}=5nm obtained by measurement and simulation. The simulation parameters for SILC calculation are the same for both devices, Huang-Rhys factor S=20, phonon energy $\hbar w_0$=0.06eV, C_0=1.5x10^{15} cm^3 sec^{-1},E_t =0.6～1.2 eV. The simulation results could be well fitted with measurements for different gate-insulator thicknesses. Figure 3 shows the measured dJ_g/J_g vs. injected hole currents Q_h with several gate bias stresses. SILC saturated at over 1x10^{-4} Q_h [C/cm^2]. We fitted each J_g vs V_g curves in order to obtain the generated trap site density N_{trap} as shown in Fig.4. It also showed good agreement. Therefore, we obtained the dependence of N_{trap} on Q_h as shown in Fig.5. It was well fitted with power law curve, $N_{trap} = 2\times10^{21}\times Q_h^{0.77}$. This dependence is the same as that in several reports. These results showed the validity of our simulation model.

3. Variability simulation

In order to reveal the origin of SILC variability, we simulated the leakage currents for different trap site distribution. Figure 6 shows the simulated Jg vs Vg curves with (a)L=1 μm,W=1 μm, (b)L=25 nm,W=25 nm nMOSFETs. The trap sites are randomly arranged in real and energy spaces for 1000 samples. The mean trap site density is N_t= 5x10^{18}cm^{-3}eV^{-1}, and trap site energy E_t=0.6-1.2eV. Small-size nMOSFETs show large variability in the low gate bias region. The median value of the small nMOSFETs is almost the same as that of the large nMOSFETs. Figure 7 shows the Gumbel plots of J_g for small-size nMOSFETs at E_{ox}=6.7MV obtained by simulation and measurement [2]. Although the simulation data was saturated at about 200 nA/cm^2, the experimental data existed more than 2μA/cm^2. These results mean that additional models are needed to enhance the SILC variability. Therefore we focused on two-step trap-assisted tunneling.

Figure 8 shows schematic diagrams of (a) one-step trap-assisted tunneling, and (b) two-step trap to trap tunneling. In order to compare the maximum probability, we arranged the trap site positions. Z_t1 are arranged at the middle of the insulator. Z_t2, Z_t3 are arranged at 1/3 and 2/3 of the insulator. In order to estimate the two-step trap-assisted tunneling currents, we use the multiphonon-transit probability MP.

$$MP(p) = \left(\frac{f_B+1}{f_B}\right)^{p/2} \exp\left[-S(2f_B+1)\right] I_m(n),$$

$$n = 2S\sqrt{f_B(f_B+1)},$$

Total probability is the product of the MP and WKB tunneling probability T. Ptt=Ttt x TTMP. Figure 9 shows the dependence of probability of each process on E_{ox}. Because the leakage currents are dominated by the lowest probability, we should focus on the Pout for one-step trap-assisted tunneling and Ptt for two-step trap-assisted tunneling currents. The trap-to-trap probability is one order higher than for one-step trap-assisted tunneling. It indicated that the two-step trap-assisted tunneling can enhance the leakage currents, and it might be the origin of the anomalous SILC.

3. Conclusion

We showed that the extended RTN model shows good agreement for the SILC measurement. In addition, we found that two-step trap-assisted tunneling currents could explain the anomalous SILC. We consider these results may lead to the comprehensive understanding of gate dielectric degradations.

References

[1] T. Nagumo et al., in IEDM Technical Digest, p.628, 2010. [2] T. Inatsuka et al., in IEEE International Reliability Physics symposium, GD.5.1, 2013. [3] K. Matsuzawa, T. Ohguro, and N. Aoki, in International Conference on Simulation of Semiconductor Processes and Devices, p.83, 2003.[4] Y. Higashi et al., in Symposium on VLSI Technology Digest of Technical Papers, p.200, 2011. [5] Y. Higashi et al., IEEE-Tranc,Elec.Dev. p.4197, 2014. [6] M. Herrmann and A. Schenk, J. Appl. Phys. **77**, p.4522, 1995.

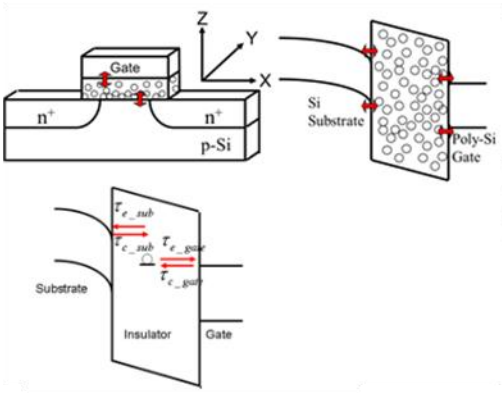

Fig. 1 Schematic of SILC model for nMOSFET. Discretized traps are arranged randomly in real and energy spaces. Electrons tunnel to the trap position via multiphonon-assisted energy transitions.

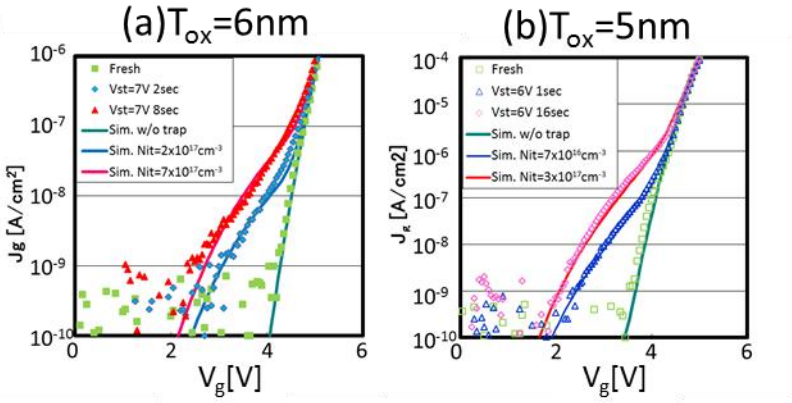

Fig. 2 Jg vs. Vg curves obtained by measurement and simulation. (a) T_{ox}=6nm, (b) T_{ox} = 5nm. The simulation parameters for SILC calculation are same for both devices, Huang-Rhys factor S=20, phonon energy $\hbar w_0$=0.06eV, C_0=1.5x10^{15} cm^3 sec^{-1}, E_t =0.6~ 1.2 eV

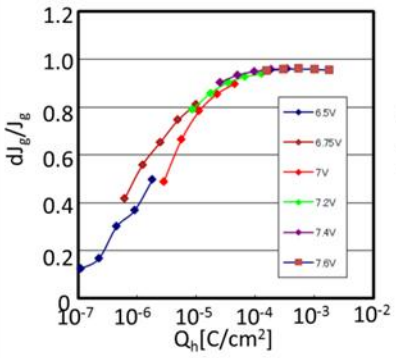

Fig. 3 Measured dJ_g/J_g vs. Q_h [C/cm^2] with several gate bias stress. T_{ox}=6nm.

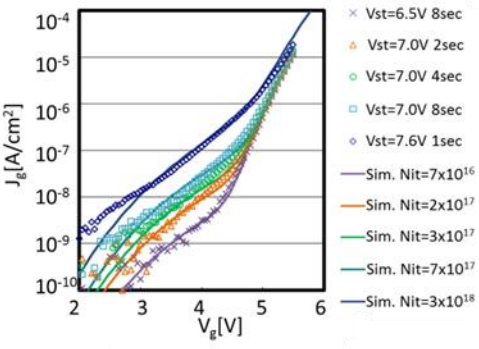

Fig. 4 Fitting results for J_g/V_g curves with several gate bias stress. T_{ox}=6nm.

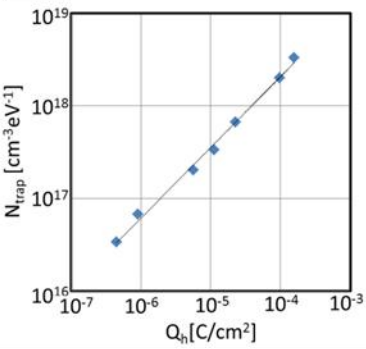

Fig. 5 Obtained N_{trap} vs. Q_h, well fitted with power low curve, $N_{trap} = 2\times 10^{21}\times Q_h^{0.77}$.

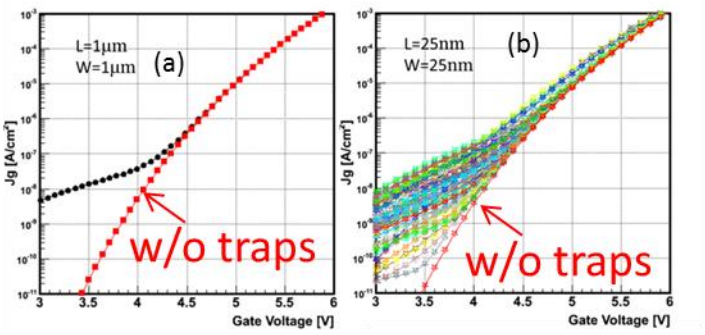

Fig. 6 Simulated J_g vs. V_g curves with (a)L=1μm,W=1μm, (b)L=25nm,W=25nm The trap sites are randomly arranged in real and energy spaces. The sample number is 1000. The mean N_t= 5x10^{18}cm^{-3}eV^{-1}, Et=0.6-1.2eV.T_{ox}=6nm.

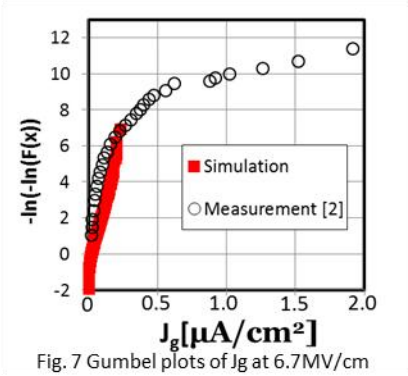

Fig. 7 Gumbel plots of Jg at 6.7MV/cm obtained by simulation. The open circle shows measurement results [2].

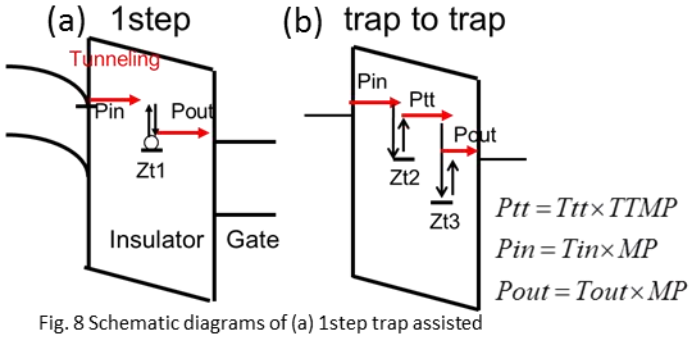

Fig. 8 Schematic diagrams of (a) 1step trap assisted tunneling, and (b) 2tep trap to trap tunneling. Zt1 are arranged at middle of the insulator. Zt2, Zt3 are arranged at 1/3 and 2/3 of T_{ox}. Et=0.8eV.

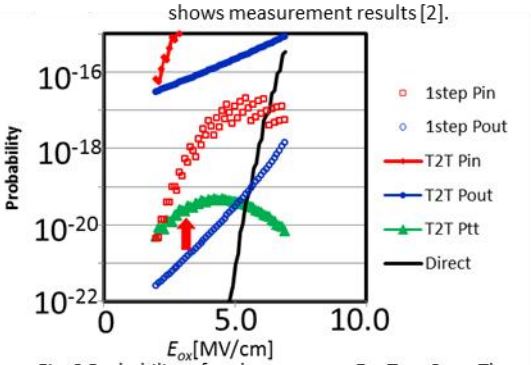

Fig. 9 Probability of each process vs. E_{ox}. Tox=6nm. The trap to trap probability is one order higher than 1step trap assisted tunneling.