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Investigation and Comparison of Quantum-Capacitance induced Inversion-Charge Loss for Ultra-Thin-Body and Double-Gate III-V n-MOSFETs

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Abstract

This work investigates and compares the intrinsic inversion capacitance (C_{inv}) of double-gate (DG) and ultra-thin-body (UTB) device structures with high-mobility $In_{0.53}Ga_{0.47}As$ channel using quantum-mechanical simulation corroborated by theoretical model calculation. Our study indicates that quantum capacitance will significantly impact the characteristics of intrinsic C_{inv} and lead to an apparent C_{inv} degradation in both device structures due to small electron effective mass of the InGaAs channel. Based on the ITRS 2018 to 2024 technology nodes, our study indicates that the mobility enhancement of the DG and UTB devices should be at least ~2.7X and ~2X, respectively, to compensate the drain-current loss due to the quantum-capacitance induced inversion-charge loss. Our study may provide insights for device designs using high-mobility III-V channel materials.

Introduction

III-V channel materials such as InGaAs are promising alternatives to Si due to small effective mass and higher carrier mobility for n-MOSFETs [1]. Although the higher permittivity makes them more susceptible to short-channel effects, it can be mitigated by ultra-thin-body (UTB) or double-gate (DG) structures. Small electron effective mass and low density-of-states (DOS) of III-V channel materials, however, may lead to quantum capacitance (C_{QM}) [2], [3], resulting in the loss of drive current because C_{QM} reduces the intrinsic inversion capacitance (C_{inv}) especially for devices with small dimensions [4].

In this work, with the aid of Poisson-Schrödinger numerical simulation corroborated by theoretical calculation, the C_{inv} degradation and the inversion-charge loss due to the impact of quantum capacitance are investigated and compared for UTB and DG InGaAs n-MOSFETs based on the ITRS 2018-2024 technology nodes (see Table I) [5].

Methodology

Figs. 1(a) and 1(b) show the schematics of UTB and DG devices in this study. Pertinent device parameters based on the ITRS 2018-2024 nodes are listed in Table I. Using coupled Poisson-Schrödinger numerical simulation [6] corroborated by theoretical model calculation, the impact of quantum capacitance on the intrinsic C_{inv} for UTB and DG devices is investigated. Fig. 2 outlines the methodology of our model calculation. The inversion charge (Q_{inv}) of the DG devices can be obtained through solving the φ_s at a given V_g with Eqs. (2) and (4) iteratively. Similarly, the Q_{inv} of the UTB devices can be obtained by Eqs. (3) and (4). The C_{inv} can then be derived by Eq. (1). Our model shows a fairly good agreement with the numerical simulation as shown in Fig. 3.

Results and Discussion

Fig. 3 shows that the C_{inv} of UTB and DG InGaAs devices possess a step-like C_{inv} vs. V_{gst} (gate-voltage overdrive) characteristic. This is a signature of the energy dependence of 2-D DOS (see Eq. (5) in Fig. 2). For a given sub-band, 2-D quantum capacitance remains a constant until the energy is high enough to reach the next sub-band. As a result, the C_{inv} exhibits a step-like behavior (Fig. 3). Since the UTB device possesses stronger electrical confinement than that of DG due to its stronger vertical electric field, the UTB device needs higher V_g to reach the second sub-band. This explains why there is only one plateau in Fig. 3(b). Fig. 4 shows the normalized C_{inv} characteristics for DG and UTB InGaAs devices with various technology nodes. It can be seen from Fig. 4(a) that the normalized C_{inv} decreases with decreasing T_{ch}.

Fig. 5 shows that the UTB device exhibits larger normalized Q_{inv} than the DG counterpart for all the technology nodes considered. This can be elucidated by Fig. 6. In Fig. 6, C_{ox} and $C_{centroid}$ can be lumped as C_{oxeff}, then the normalized C_{inv} of UTB and DG devices can be expressed as $C_{inv}^{-1} = C_{oxeff}^{-1} + C_{QM}^{-1}$ and $C_{inv}^{-1} = C_{oxeff}^{-1} + 2(C_{QM}^{-1})$, respectively. This explains why, for a given T_{ch}, the normalized C_{inv} (and thus the normalized Q_{inv}) of the UTB InGaAs device is larger than the DG counterpart (Fig. 5).

Fig. 7 shows that there are no step-like characteristics for both the UTB and DG Si devices. Namely, the impact of quantum capacitance is negligible for Si devices due to its large effective mass [7]. Figs. 8(a) and 8(b) show the Q_{inv} ratio of Si to InGaAs channel ($Q_{inv,Si}/Q_{inv,InGaAs}$) for DG and UTB devices, respectively, with various technology nodes. It indicates that the mobility enhancement of the InGaAs devices should be at least ~2.7X for DG structures and ~2X for UTB structures for compensating the excess inversion-charge loss due to quantum capacitance. Note that, if the T_{ch} of the UTB device is one half that of the DG one (with comparable device electrostatics), the required mobility enhancement of the UTB device (~1.8X) is also lower than that of the DG device.

Acknowledgement

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Table I. Pertinent device parameters from ITRS 2018-2024 nodes [5]

Year	2018	2021	2024
T_{ch}	8.5nm	6.1nm	4nm
EOT	0.68nm	0.59nm	0.5nm

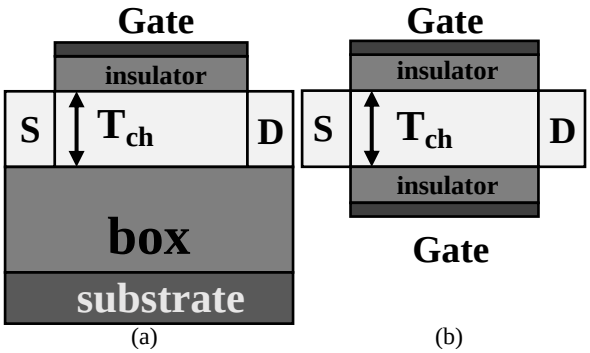

Fig. 1 (a) UTB, and (b) DG structures used in this study. T_{ch} is the channel thickness. The buried-oxide (box) thickness of the UTB device is 10nm.

$$C_{inv} = \frac{dQ_{inv}}{dV_g} \quad (1)$$

For double-gate devices:

$$Q_{inv} = 2C_{oxeff} \cdot (V_g - V_{FB} - \varphi_s) \quad (2)$$

For ultra-thin body devices:

$$Q_{inv} = C_{oxeff} \cdot (V_g - V_{FBfg} - \varphi_s) + C_{boxeff} \cdot (V_{sub} - V_{FBbg} - \varphi_s) \quad (3)$$

$$Q_{inv} = q\sum_i \int_{E_{min,i}}^{\infty} DOS_{2-D}(E) \cdot \frac{1}{1+\exp(\frac{E-E_f}{kT})} dE = \frac{qm_{ch}^* kT}{\pi\hbar^2} \sum_i \ln\left[1+\exp(\frac{\varphi_s - \frac{E_i}{q} - \frac{E_g}{q}}{V_T})\right] \quad (4)$$

$$DOS_{2-D} = i \cdot \frac{m_{ch}^*}{\pi\hbar^2} \quad (5)$$

Fig. 2 Model methodology of C_{inv}. C_{oxeff} and C_{boxeff} have considered the impact of the centroid capacitance. V_{FB}, V_{FBfg} and V_{FBbg} are the flat-band voltages. V_{sub} is the substrate bias (ground plane) of the UTB devices. φ_s is the potential at carrier centroid. m_{ch}^* is the electron effective mass. E_i is the i^{th} sub-band eigen-energy. E_i can be calculated [2].

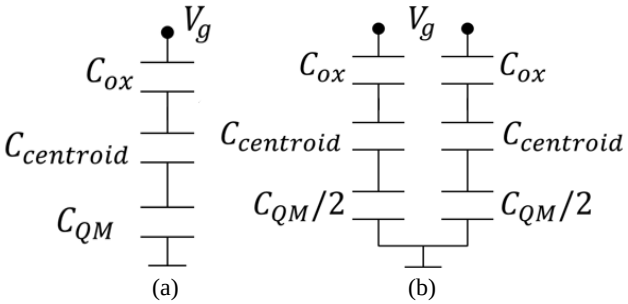

Fig. 6 Inversion capacitance models for (a) UTB, and (b) DG devices.

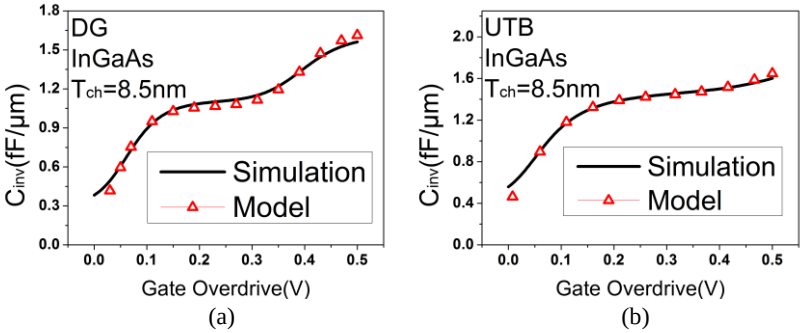

Fig. 3 Simulated and modeled C_{inv} (normalized with total width) for (a) DG, and (b) UTB InGaAs devices with the 2018 technology node.

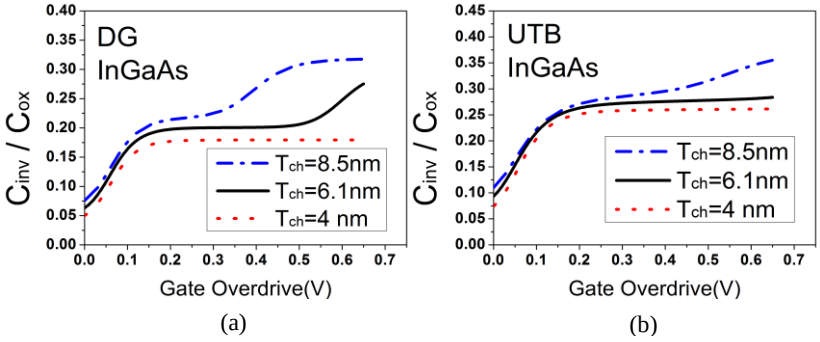

Fig. 4 Normalized C_{inv} of (a) DG, and (b) UTB InGaAs devices with various technology nodes (Table I).

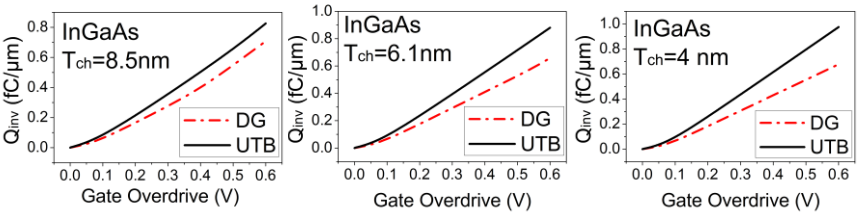

Fig. 5 Comparison of Q_{inv} (normalized with total width) between DG and UTB InGaAs devices for various technology nodes (Table I).

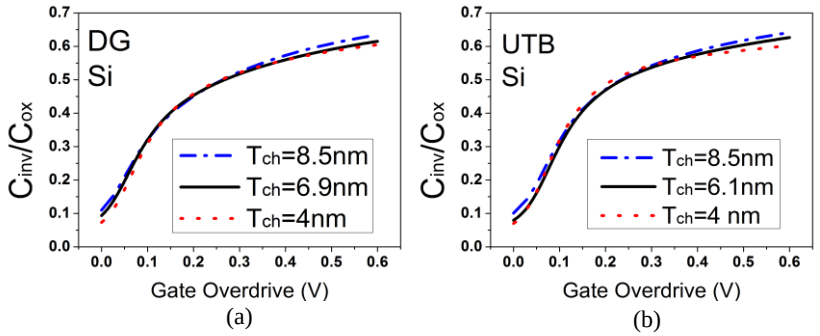

Fig. 7 Normalized C_{inv} of (a) DG, and (b) UTB Si devices with various technology nodes (Table I).

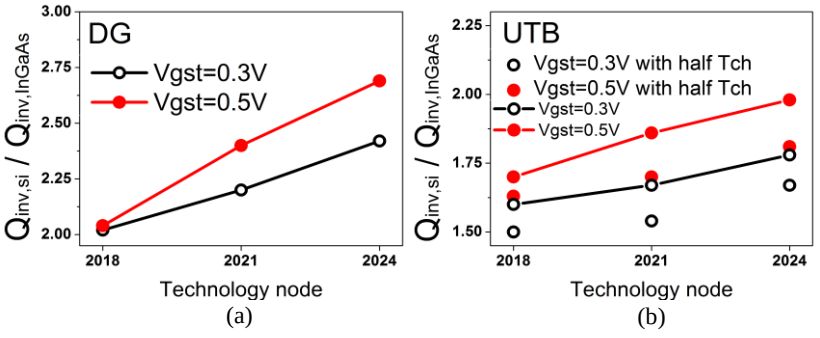

Fig. 8 Q_{inv} ratio of Si to InGaAs channel for (a) DG, and (b) UTB devices with various technology nodes (Table I).