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Improved Interface of HfO2/InGaAs MOS by Employing Thin SiNx Interfacial Layer Using Plasma Enhanced Atomic Layer Deposition

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Abstract

In this paper, a new method to improve HfO_2 /InGaAs interface is studied. Ultra-thin SiN_x deposited by using PEALD technique shows enhanced performance in both C-V_G and I_D-V_G characteristics. 1.5nm CET InGaAs MOS quantum well FET using SiN_x interfacial layer is demonstrated. We suggest ultra-thin PEALD SiN_x as a promising candidate for improvement of the high-k/III-V interface quality and further EOT scaling.

1. Introduction

As logic transistors continue to scale down, III-V MOS devices have emerged as post-Si transistors due to their superior transport properties, and remarkable developments have been achieved over the past two decades [1]. However, the lack of high quality native insulator which is the major bottleneck of III-V materials has prohibited the improvement of III-V MOS quality. Recently, many studies have mainly focused on the high-k/InGaAs interface.

To improve the interface properties, only optimizing the high-k dielectric deposition is not enough and thus other approaches have been performed. Insertion of Al_2O_3 inter-layers between HfO_2 and InGaAs has been reported and demonstrated excellent InGaAs MOS quality [2]. However, these approaches suffer from surface oxidation due to oxygen-based dielectric deposition, which makes it hard to control the interface properties. Fine electrical properties of SiN_x/InGaAs MOS were reported [3]. Recently, we also reported excellent characteristics of PEALD SiN_x/InGaAs MOS [4], but the use of SiN_x as an interfacial layer has been failed for further EOT scaling.

In this work, we suggest an ultra-thin SiN_x as the interfacial layer between HfO_2 and InGaAs interface by using plasma enhanced atomic layer deposition (PEALD) technique. By using PEALD method, precise control of SiN_x thickness and in-situ N_2 plasma nitridation, which improves the interface quality, are possible. As a result, we have demonstrated HfO_2/SiN_x/InGaAs MOS devices with enhanced interface properties.

2. Experiment

In order to study the effects and the optimization of the ultra-thin SiN_x interfacial layer on HfO_2/InGaAs interface, we fabricated InGaAs MOS capacitors with various thickness (none, 0.1, 0.2, and 0.5 nm) of SiN_x inter-layer with 12.3 nm thick HfO_2. Epitaxial structure of the wafer for MOS capacitors is composed of Si doped n-type $In_{0.53}Ga_{0.47}As$ channel layer with a doping concentration of 1.0E+17 /cm^3 which is grown on InP substrate. Before insulator deposition, wafer cleanings using acetone, diluted HCl, and NH_4OH (29%) solutions were performed to remove native oxides on the surface. Ultra-thin SiN_x interfacial layer was deposited at 400 ℃ in ICP-CVD chamber. PEALD technique was employed with SiH_4 and N_2. The deposition rate of PEALD SiN_x process was approximately 0.25 Å/cycle. Bulk HfO_2 layer was deposited at 360 ℃ in ALD chamber using $Hf[N(C_2H_5)(CH_3)]_4$ (TEMAH) and O_3 as precursors. The deposition rate of ALD HfO_2 was approximately 0.9 Å/cycle. Both gate metal (Pt/Au) and bottom metal (Ti/Au) were deposited using e-beam evaporation. Finally, post-metal-annealing (PMA) at 400 ℃ for 10 min in forming gas ambient (N_2 95%, H_2 5%) was carried out. The results for MOS capacitors are shown in Fig. 1.

After optimizing the gate dielectric (SiN_x 0.2 nm / HfO_2 3 nm), long channel InGaAs quantum well FET was fabricated. The epitaxial structure of the wafer is composed of InP substrate, $In_{0.52}Al_{0.48}As$ buffer 400 nm, Si-delta doping below the 10 nm $In_{0.7}Ga_{0.3}As$ channel, 2 nm InP etch stop and 55 nm InGaAs capping layer with doping concentration of 5.0E+19 /cm^2. First, mesa isolation was performed using BCl_3/Cl_2 based plasma etching. Then, gate recess was done by citric acid using a SiN_x mask. To further etch the InP etch stop layer, HCl based digital etching were performed. As a pre-treatment before dielectric deposition, 3 min in NH_4OH (29%) was performed. Gate insulator was deposited with the same condition described in the above. 0.2 nm SiN_x (8 cycles of PEALD) and 3 nm of ex-situ HfO_2 (33 cycles of ALD) were deposited. Ohmic metal (Mo/Au) and gate metal (Pt/Au) were both deposited using e-beam evaporation. Finally, PMA was carried out at 400 ℃ for 30 min in forming gas ambient (N_2 95%, H_2 5%). The gate length and width of the fabricated devices were 2 μm and 50 μm, respectively. The results are shown in Fig. 2 and Fig. 3.

3. Results and Discussions

C-V_G characteristics of HfO_2/InGaAs MOS capacitor with various thickness of interfacial SiN_x were investigated.

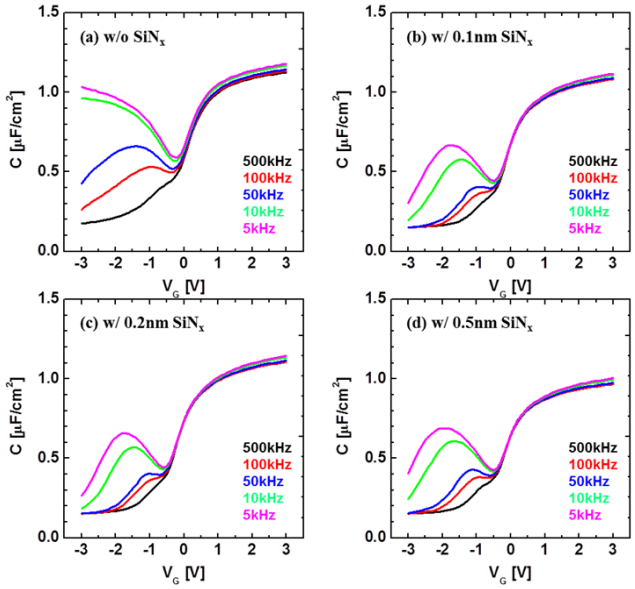

Fig. 1 C-V_G characteristics of HfO_2/InGaAs MOS capacitor with different thickness of SiN_x of (a) none, (b) 0.1 nm, (c) 0.2 nm, and (d) 0.5 nm.

Significant effects of ultra-thin SiN_x interfacial layer in C-V_G characteristics were observed. Without SiN_x inter-layer, large frequency dispersion phenomenon occurred, which indicated poor interface quality. In contrast, with only 0.1 nm of SiN_x, frequency dispersion in the accumulation, depletion regions, and weak-inversion hump were significantly improved. This is attributed to lower interface traps and border traps with SiN_x interlayer existence [5]. With 0.2 nm of SiN_x, further improvement was observed. However, no enhancement occurred with thicker SiN_x deposition. We suggest that the surface nitridation effect during PEALD step may clean and passivate the surface defect and result in better interface quality [6]. Also, SiN_x may effectively block the oxygen source during HfO_2 ALD, meaning less native oxides. Moreover, border traps, another important interface property, were greatly improved, which suggests that 0.2 nm of high quality PEALD SiN_x may be enough to screen out the border trap in HfO_2.

I_D-V_G characteristics of the fabricated 1.5 nm CET InGaAs MOS quantum well FET with and without SiN_x inter-layer are shown in Fig. 2. Solid and broken curves indicate the transfer curves obtained by sweeping the voltage positively and negatively, respectively. With SiN_x inter-layer, hysteresis decreases and $G_{m(max)}$ was increased from 174 to 243 μS/μm. Also, the subthreshold swing (SS) was improved from 150 to 100 mV/decade. Drain induced barrier lowering current also was improved from 180 to 100 mV/V.

C-V_G characteristics of the fabricated 1.5 nm CET InGaAs MOS quantum well FET with and without SiN_x inter-layer are shown in Fig. 3. It clearly shows that frequency dispersions are effectively suppressed with SiN_x inter-layer, also in the CET of 1.5 nm.

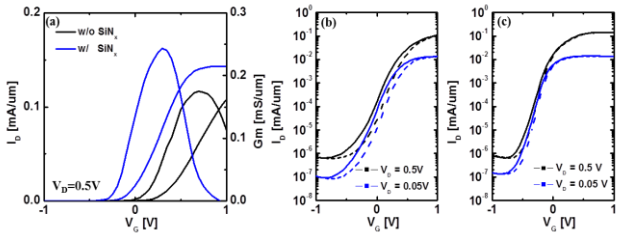

Fig. 2 I_D-V_G characteristics of 1.5 nm CET InGaAs MOS QW FET (a) with and without SiN_x at V_D=0.5 V, (b) without SiN_x (log-scaled), and (c) with SiN_x (log-scaled).

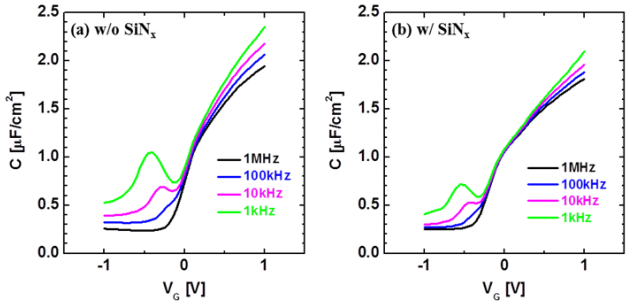

Fig. 3 C-V_G characteristics of 1.5 nm CET InGaAs MOS QW FET (a) without SiN_x and (b) with SiN_x.

These results are consistently indicating that ultra-thin SiN_x insertion improves the interface of HfO_2/InGaAs and show the potential of SiN_x interfacial layer for scaled-down III-V MOS devices.

4. Conclusions

Investigations on the impact of ultra-thin SiN_x for HfO_2 /InGaAs MOS interface were studied. With 0.2 nm SiN_x inter-layer, frequency dispersions were significantly reduced. Also, 1.5 nm CET InGaAs MOS devices were successfully demonstrated using the SiN_x interfacial layer. We expect that SiN_x could be a solution for further-EOT-scaled and short channel InGaAs MOS devices.

Acknowledgements

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