Improved Interface of HfO2/InGaAs MOS by Employing Thin SiNx Interfacial Layer Using Plasma Enhanced Atomic Layer Deposition

Su-Keun Eom¹, Ra-Seong Ki¹, Dong-Hwan Kim¹, Ho-Young Cha², and Kwang-Seok Seo¹

¹Department of Electrical and Computer Engineering and Inter-University Semiconductor Research Center, Seoul National University, Seoul 151-744, Republic of Korea
²School of Electronic and Electrical Engineering, Hongik University, Seoul 121-791, Republic of Korea
E-mail: ¹ksseo@snu.ac.kr

Abstract
In this paper, a new method to improve HfO₂/InGaAs interface is studied. Ultra-thin SiNₓ deposited by using PEALD technique shows enhanced performance in both C-V and Iₚ-Iₚ₇ characteristics. 1.5nm CET InGaAs MOS quantum well FET using SiNₓ interfacial layer is demonstrated. We suggest ultra-thin PEALD SiNₓ as a promising candidate for improvement of the high-k/III-V interface quality and further EOT scaling.

1. Introduction
As logic transistors continue to scale down, III-V MOS devices have emerged as post-Si transistors due to their superior transport properties, and remarkable developments have been achieved over the past two decades [1]. However, the lack of high quality native insulator which is the major bottleneck of III-V materials has prohibited the improvement of III-V MOS quality. Recently, many studies have mainly focused on the high-k/InGaAs interface.

To improve the interface properties, only optimizing the high-k dielectric deposition is not enough and thus other approaches have been performed. Insertion of Al₂O₃ inter-layers between HfO₂ and InGaAs has been reported and demonstrated excellent InGaAs MOS quality [2]. However, these approaches suffer from surface oxidation due to oxygen-based dielectric deposition, which makes it hard to control the interface properties. Fine electrical properties of SiNₓ/InGaAs MOS were reported [3]. Recently, we also reported excellent characteristics of PEALD SiNₓ/InGaAs MOS [4], but the use of SiNₓ as an interfacial layer has been failed for further EOT scaling.

In this work, we suggest an ultra-thin SiNₓ as the interfacial layer between HfO₂ and InGaAs interface by using plasma enhanced atomic layer deposition (PEALD) technique. By using PEALD method, precise control of SiNₓ thickness and in-situ N₂ plasma nitridation, which improves the interface quality, are possible. As a result, we have demonstrated HfO₂/SiNₓ/InGaAs MOS devices with enhanced interface properties.

2. Experiment
In order to study the effects and the optimization of the ultra-thin SiNₓ interfacial layer on HfO₂/InGaAs interface, we fabricated InGaAs MOS capacitors with various thickness (none, 0.1, 0.2, and 0.5 nm) of SiNₓ inter-layer with 12.3 nm thick HfO₂. Epitaxial structure of the wafer for MOS capacitors is composed of Si doped n-type In₀.₅₃Ga₀.₄₇As channel layer with a doping concentration of 1.0E+17/cm³ which is grown on InP substrate. Before insulator deposition, wafer cleanings using acetone, dilute HCl, and NH₄OH (29%) solutions were performed to remove native oxides on the surface. Ultra-thin SiNₓ interfacial layer was deposited at 400 °C in ICP-CVD chamber.

PEALD technique was employed with SiH₄ and N₂. The deposition rate of PEALD SiNₓ process was approximately 0.25 Å/cycle. Bulk HfO₂ layer was deposited at 360 °C in ALD chamber using Hf[N(CH₃)₂]₄ (TEMAH) and O₂ as precursors. The deposition rate of ALD HfO₂ was approximately 0.9 Å/cycle. Both gate metal (Pt/Au) and bottom metal (Ti/Au) were deposited using e-beam evaporation. Finally, post-metal-annealing (PMA) at 400 °C for 10 min in forming gas ambient (N₂ 95%, H₂ 5%) was carried out. The results for MOS capacitors are shown in Fig. 1.

After optimizing the gate dielectric (SiNₓ 0.2 nm / HfO₂ 3 nm), long channel InGaAs quantum well FET was fabricated. The epitaxial structure of the wafer is composed of InP substrate, In₀.₅₂Al₀.₄₈As buffer 400 nm, Si-delta doping below the 10 nm In₀.₅₃Ga₀.₄₇As channel, 2 nm InP etch stop and 55 nm InGaAs capping layer with doping concentration of 5.0E+19/cm³. First, mesa isolation was performed using BCl₃/Cl₂ based plasma etching. Then, gate recess was done by citric acid using a SiNₓ mask. To furtheretch the InP etch stop layer, HCl based digital etching were performed. As a pre-treatment before dielectric deposition, 3 min in NH₄OH (29%) was performed. Gate insulator was deposited with the same condition described in the above. 0.2 nm SiNₓ (8 cycles of PEALD) and 3 nm of ex-situ HfO₂ (3 cycles of ALD) were deposited. Ohmic metal (Mo/Au) and gate metal (Pt/Au) were both deposited using e-beam evaporation. Finally, PMA was carried out at 400 °C for 30 min in forming gas ambient (N₂ 95%, H₂ 5%). The gate length and width of the fabricated devices were 2 μm and 50 μm, respectively. The results are shown in Fig. 2 and Fig. 3.

3. Results and Discussions
C-V characteristics of HfO₂/InGaAs MOS capacitor with various thickness of interfacial SiNₓ were investigated.

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Significant effects of ultra-thin SiN\textsubscript{x} interfacial layer in C-V\textsubscript{G} characteristics were observed. Without SiN\textsubscript{x} inter-layer, large frequency dispersion phenomenon occurred, which indicated poor interface quality. In contrast, with only 0.1 nm of SiN\textsubscript{x}, frequency dispersion in the accumulation, depletion regions, and weak-inversion hump were significantly improved. This is attributed to lower interface traps and border traps with SiN\textsubscript{x} interlayer existence [5]. With 0.2 nm of SiN\textsubscript{x}, further improvement was observed. However, no enhancement occurred with thicker SiN\textsubscript{x} deposition. We suggest that the surface nitridation effect during PEALD step may clean and passivate the surface defect and result in better interface quality [6]. Also, SiN\textsubscript{x} may effectively block the oxygen source during HfO\textsubscript{2} ALD, meaning less native oxides. Moreover, border traps, another important interface property, were greatly improved, which suggests that 0.2 nm of high quality PEALD SiN\textsubscript{x} may be enough to screen out the border trap in HfO\textsubscript{2}.

$I_{D}$-$V_{G}$ characteristics of the fabricated 1.5 nm CET InGaAs MOS quantum well FET with and without SiN\textsubscript{x} inter-layer are shown in Fig. 2. Solid and broken curves indicate the transfer curves obtained by sweeping the voltage positively and negatively, respectively. With SiN\textsubscript{x} inter-layer, hysteresis decreases and $G_{m(max)}$ was increased from 174 to 243 $\mu$S/μm. Also, the subthreshold swing (SS) was improved from 150 to 100 mV/decade. Drain induced barrier lowering current also was improved from 180 to 100 mV/V.

C-V\textsubscript{G} characteristics of the fabricated 1.5 nm CET InGaAs MOS quantum well FET with and without SiN\textsubscript{x} inter-layer are shown in Fig. 3. It clearly shows that frequency dispersions are effectively suppressed with SiN\textsubscript{x} inter-layer, also in the CET of 1.5 nm.

These results are consistently indicating that ultra-thin SiN\textsubscript{x} insertion improves the interface of HfO\textsubscript{2}/InGaAs and show the potential of SiN\textsubscript{x} interfacial layer for scaled-down III-V MOS devices.

4. Conclusions
Investigations on the impact of ultra-thin SiN\textsubscript{x} for HfO\textsubscript{2}/InGaAs MOS interface were studied. With 0.2 nm SiN\textsubscript{x} inter-layer, frequency dispersions were significantly reduced. Also, 1.5 nm CET InGaAs MOS devices were successfully demonstrated using the SiN\textsubscript{x} interfacial layer. We expect that SiN\textsubscript{x} could be a solution for further-EOT-scaled and short channel InGaAs MOS devices.

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References