Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp558-559

Behavior of the Potential-Induced Degradation for Photovoltaic Modules Fabricated Using Flat Mono-Crystalline Silicon Cells with Different Surface Orientations

Seira Yamaguchi[1], Atsushi Masuda[2] and Keisuke Ohdaira[1]

[1] Japan Advanced Institute of Science and Technology (JAIST)
1-1, Asahidai, Nomi, Ishikawa 923-1292, Japan
E-mail: s-yamaguchi@jaist.ac.jp
[2] National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan

Abstract

This paper deals with the behavior of the potential-induced degradation (PID) of photovoltaic modules fabricated using p-type flat mono-crystalline silicon cells with (100) and (111) surface orientations. PID tests are performed by applying a voltage of −1000 V to connected interconnector ribbons of the modules. A decrease in the normalized maximum power of the modules with (100)-oriented cells is more significant than that with (111)-oriented cells, implying that the (111)-oriented cells have the higher PID resistance.

1. Introduction

Photovoltaic (PV) modules in very large-scale (VLS) PV systems often suffer from potential-induced degradation (PID). PID for crystalline silicon (c-Si) modules can be attributed to alkali metals, e.g. sodium, migrating from module cover glass due to high system voltages [1]. Recently, it has been shown that groove-rounded-textured cells, which partially have (100) surface, show relatively high PID-resistance, compared with the cells with standard textured surface [2]. Their findings indicate that PID may have a dependence on surface orientations. In this study, we have investigated the dependence of PID on the surface orientation.

2. Method

2.1 Cell and module fabrication

(100)- or (111)-oriented, one-side polished p-type c-Si wafers were cleaved to 20 × 20 mm^2-sized substrates. The front surface of the substrates was coated with liquid phosphorus silicate glass source by spin coating, and the substrates were subsequently annealed at 850 °C in N_2 atmosphere in order to form n^+ emitters. The emitters on the flat c-Si surfaces had a sheet resistance of ~30 Ω/sq. After the removal of the phosphorus silicate glass remaining on the c-Si surfaces, SiN_x antireflection coatings with a thickness of ~70 nm were deposited onto the n^+ emitter surfaces by catalytic chemical vapor deposition. Ag and Al pastes were printed onto the front and rear surfaces of the c-Si substrates by screen printing, followed by firing at a peak temperature of 800 °C under air atmosphere in a tube furnace.

Interconnector ribbons were soldered onto cell's front and rear Ag contacts. Stacks composed of cover glass/ethylene-vinyl acetate copolymer (EVA) encapsulant/c-Si cell/EVA encapsulant/typical backsheet were prepared. The cover glass has a size of 45 × 45 mm^2 and contains alkali metals such as sodium. The modules were fabricated from the stacks in a module laminator. Our lamination process had two steps: degassing step for 5 min and adhesion step for 15 min. The stacks were placed with the cover glass side down on the heater maintained at 135 °C during lamination.

2.2 PID tests and characterization

PID tests were performed by applying a voltage of −1000 V to shorted module contacts using an Al plate placed on the cover glass of modules at 85 °C. We use the term "PID stress" here to refer to such voltage and temperature stress. In order to evaluate the degradation, current density–voltage (*J–V*) measurements were conducted under dark and 1-sun-illuminated conditions for the modules before and after the PID tests. Saturation current density J_0, parallel resistance R_p, and ideality factor n were determined by fitting the dark *J–V* data to the following single-diode equation:

$$J(V) = J_0\left[\exp\left(\frac{q(V - JR_s)}{nkT}\right) - 1\right] + \frac{V - JR_s}{R_p}, \qquad (1)$$

where q is elementary charge, R_s series resistance, k Boltzmann constant, and T absolute temperature. Here, we did not restrict n to ≤ 2.

3. Results and Discussion

Figure 1 shows the dependence of the normalized maximum power $P_{max}/P_{max,0}$ of the modules fabricated using (100) and (111) cells on PID-stress duration, where P_{max} is maximum power, and $P_{max,0}$ is initial maximum power. As can be seen in Fig. 1, the $P_{max}/P_{max,0}$ of both (100) and (111) modules decreases with PID-stress duration, demonstrating that PID occurs regardless of surface orientations. The decrease in $P_{max}/P_{max,0}$ of the modules with (100)-oriented cells is, however, more significant than that of the modules with (111)-oriented cells. This implies that the PID behavior of p-type c-Si modules depends on the surface orientation of the cells, and cells with (111) surface orientations have higher PID resistance than that with (100) surface orientations.

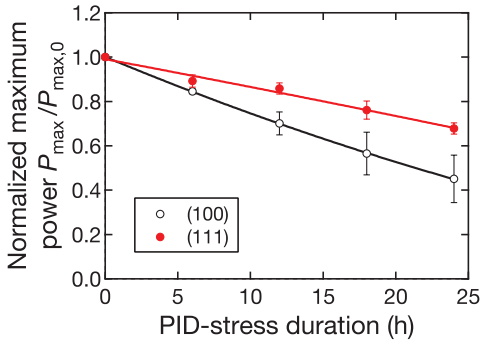

Fig. 1. Dependence of $P_{max}/P_{max,0}$ of the modules with (100)- and (111)-oriented cells on PID-stress duration. Each data point shows the mean value for three modules, and each error bar corresponds to the standard error of the mean.

Figure 2 shows the dependence of J_0, n, and $1000/R_p$ of the modules with (100) and (111) cells on PID-stress duration. All J_0, n, and $1000/R_p$ of the (100) modules are significantly increased by PID-stress, compared with those of the (111) modules. In particular, inverse R_p shows clear dependence on the surface orientation of cells. This indicates that cells with (111) surface tend to be less influenced by shunts caused by PID stress. PID-affected modules show significantly high n values (exceeding 2), as displayed in Fig. 2. These significantly high n values have been observed in PID of c-Si PV modules [3] and originate from a significantly high defect density in the depletion region introduced by PID stress [4].

It has been reported that PID shunts originate from Na-decorated intrinsic stacking faults penetrating the n^+ emitter of solar cells [4]. Based on this fact, PID behavior can be influenced by the number of such stacking faults. First, we should therefore consider the depth of pn junction formed by the phosphorus diffusion process. We were not able to observe a clear difference between the values of sheet resistance of n^+ emitters on (100) and (111) substrates. In addition, it has been reported that the diffusion coefficients of P in Si(100) and Si(111) are almost the same [5]. These suggest that the junction depth is independent of surface orientation, and that we should discuss other effects.

We consider the number of intrinsic stacking faults in unaffected cells as the second candidate. One lattice point is included in four {111}-related planes. In (100) substrates, these four types of planes can penetrate the pn junction. On the other hand, in (111) substrates, one of the four planes does not penetrate the pn junction, since the plane is parallel to the front surface. Assuming that the intrinsic stacking faults occur with the same probability per {111}-related plane, this might suggest the fewer number of PID-related stacking fault in (111) cells than that in (100) cells. Much additional work is required for the complete understanding of this phenomenon.

4. Conclusions

We have investigated the dependence of PID on the cell surface orientations. The results demonstrate that inverse R_p of the (100) cells is significantly increased by PID-stress, compared with those of the (111) modules. This suggests that (111) cells have higher PID resistance.

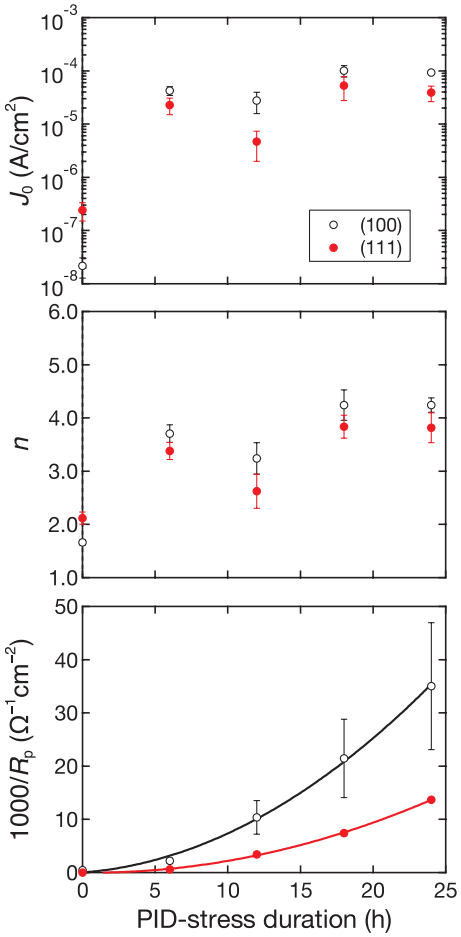

Fig. 2. Dependence of J_0, n, and $1000/R_p$ of the modules with (100)- and (111)-oriented cells on PID-stress duration. Each data point shows the mean value for three modules, and each error bar corresponds to the standard error of the mean.

Acknowledgements

This work was partially supported by NEDO. The authors would like to acknowledge Dr. Kohjiro Hara and Sachiko Jonai of AIST for their advice about the module lamination. We would also like to thank Chie Yamamoto of JAIST for her assistance.

References

[1] P. Hacke, M. Kempe, K. Terwilliger, S. Glick, N. Call, S. Johnston, S. Kurtz, I. Bennett, and M. Kloos, *Proc. 25th European Photovoltaic Solar Energy Conf. Exhib.* (2010) 3760.

[2] Y.-C. Chen C.-C. Wang, S.-H. Yang, Y.-H. Wang, C.-T. Tsai, K.-C. Lin, G.-F. Chen, and W. K. W. Huang, presented at *2014 NREL Photovoltaic Module Reliability Workshop* (2014).

[3] M. Schütze M. Junghänel, O. Friedrichs, R. Wichtendahl, M. Scherff, J. Müller, and P. Wawer, *Proc. 26th European Photovoltaic Solar Energy Conf. Exhib.* (2011) 3097.

[4] V. Naumann D. Lausch, A. Hähnel, J. Bauer, O. Breitenstein, A. Graff, M. Werner, S. Swatek, S. Großer, J. Bagdahn, and C. Hagendorf, Sol. Energy Mater. Sol. Cells **120** (2014) 383.

[5] T. C. Chan and C. C. Mai, Proc. IEEE **58** (1970) 588.