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Improving Step Coverage of PVD Barrier/Seed through Bias Power Alternation for High Aspect Ratio TSVs

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Abstract

Continuous and conformal barrier/seed layers are critical for voids free copper plating and reliable TSV interconnection. In this paper, we use the common industrial method of PVD to deposit barrier/seed layers in our 10x100μm TSV interposer process. A process optimization method of alternately using high bias power and low bias power was adopted to improve the step coverage of barrier/seed layers. Thanks to this improvement, voids free Cu electroplating in the 10x100μm TSV across a 300mm wafer is successfully achieved.

1. Introduction

The barrier/seed layers for Cu electroplating play a critical role in the realization of TSVs. Physical Vapor Deposition (PVD) is still the preferred method for depositing these films. However, the step coverage of PVD process is low, particularly on the recessed features[4]. Therefore, thick barrier/seed layers on the field are necessary to guarantee the position with thinnest metal layer can survive in the plating bath, which brings additional CMP cost and serious overhang negative to electroplating.

In this paper, a developed method that alternately using low bias power and high bias power is adopted to improve the step coverage of barrier/seed layer. With the optimized process, void free electroplating in high aspect ratio TSVs is achieved using thinner barrier/seed layers.

2. Experiments

The experimental samples are fabricated on 300mm p-type wafers. The targeted TSVs have a 100μm depth and a 10μm diameter, i.e. aspect ratio (AR)=10. Within the TSV module, 2um TEOS (tetraethyl orthosilicate) deposited by PECVD or 400nm thermal oxide is formed on the Si sidewall after Si Bosch etch. Afterwards, barrier and seed layers, Ti and Cu used in the study, are deposited with Polaris T430 PVD system. This PVD tool has distinguishing designed magnetron for magnetic confinement. Combined with high DC power(i.e. 38KW) and low process pressure(<1mTorr), the flux of metal species with high level of ionization is achieved, which is a basic premise of process optimization method introduced here.

The step coverage of metal layers was measured with SEM. The cross-section samples of SEM were prepared by ultra-fine grinding or FIB after epoxy casting. The continuousness is checked by TEM or void free electroplating which is confirmed by X-Ray and SEM cross-section measurements.

3. Results and discussions

Our baseline PVD deposition process was applied to TSV with AR=10, obvious incomplete filling at TSV's bottom is observed after plating, as shown in Fig.1.

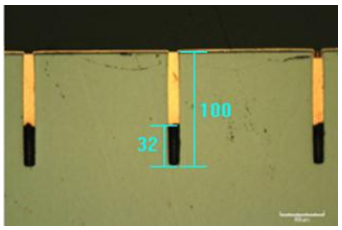

Fig. 1 The result of electroplating of 10x100μm TSVs with baseline PVD process.

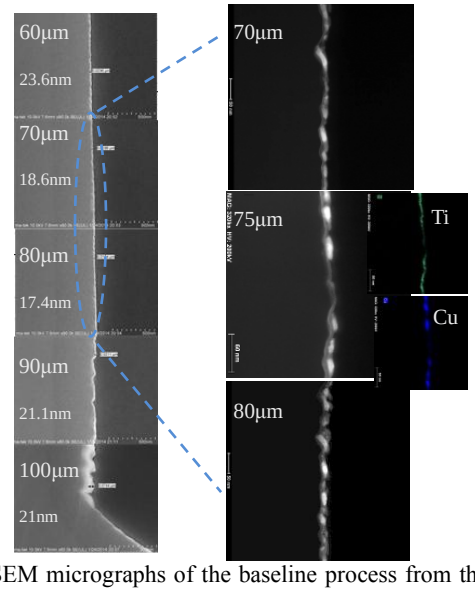

Fig. 2 SEM micrographs of the baseline process from the area of 60μm to bottom corner (left column of graphs), TEM micrographs of weakest area of 70μm to 80μm(right column of graphs)and EDX mapping of the position around 75μm(the right inserts).

In general, incomplete copper filling is caused by discontinuous seed layer on the sidewall of vias, and the failure point is corresponding to the weakest area of seed layer. This is confirmed by SEM and TEM measurement indicated in Fig.2.

Considering the weakest point of seed layer located in the lower part of vias, high bias power with narrow angular distribution and higher energy ions was applied to the 10x100μm TSV wafer with thermal oxide liner, aiming to increase the step coverage of this area. To exclude the influencing factors of field thickness, step coverage information compared with baseline process' are summarized in table 1. The corresponding results of SEM micrographs is indicated in Fig.3.

Table I The step coverage information of baseline process and high bias power process

test position (μm)	baseline with low bias power		high bias power		step coverage improvement
	thickness (nm)	step coverage	thickness (nm)	step coverage	
field	1171		1420		
40	49.6	4.24%	43.4	3.06%	-1.18%
50	38.4	3.28%	38.4	2.70%	-0.57%
60	23.6	2.02%	27.3	1.92%	-0.09%
70	18.6	1.59%	31	2.18%	0.60%
80	17.4	1.49%	42.2	2.97%	1.49%
90	21.1	1.80%	62	4.37%	2.57%
100	112	9.56%	190	13.4%	3.82%
Cor.	20	1.71%	0	0%	-1.71%
Bot.	132.4	11.3%	106	7.47%	3.84%

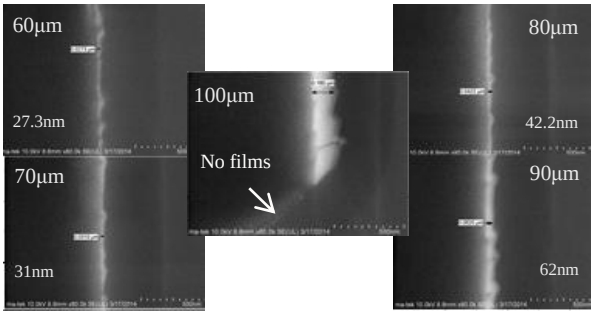

Fig.3 SEM micrographs of the process with high bias power corresponding to the area of 60μm to bottom corner.

According to the results mentioned above, the step coverage of 70μm to 90μm area of via sidewalls, which is the thinnest area of TSVs, are all get improved. However, the metal thickness of the bottom corner reduced down to 0, which will be a failure point in subsequent plating process.

Moreover, we also find that high step coverage at middle sidewall and bottom corner is acquired with baseline process. That is to say, as bias power decreases, the step coverage of these areas increases. It is not difficult to find a process window with step coverage at middle sidewall and bottom corner high enough to meet the requirement of plating process. Therefore, an optimized process method is the combination of low bias power chosen in the process window and high bias power mentioned above. It will take advantages of strong points of the two processes and will be the best way to achieve continuous metal layers with high step coverage.

Finally, the optimized process is employed on TSV wafers with thermal liner and TEOS liner, and the thickness of the seed layer is reduced down to 1.5μm. Wafer level voids free plating is realized on both types of wafer, which is confirmed by 9 points X-Ray measurement and SEM cross-section micrographs.

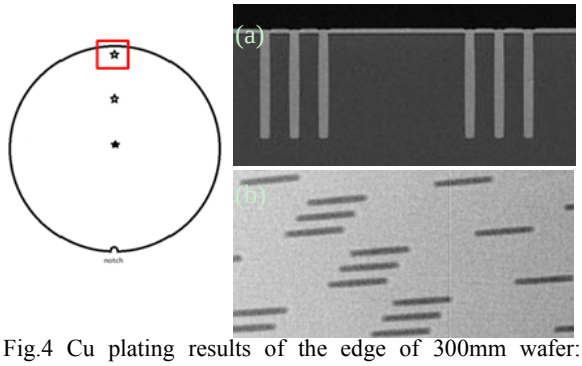

Fig.4 Cu plating results of the edge of 300mm wafer: SEM cross-section micrograph (a) and X-Ray image(b).

4. Conclusions

By comparing the step coverage performance of low bias power and high bias power, we find that high bias power could improve step coverage of the lower part of vias sidewalls but sputter the bottom corner to no films, while the process of low bias power obtains high step coverage of bottom corner and middle sidewall. By alternately applying the two types of power on the substrate, step coverage and conformality of barrier and seed layer are all get improved. With the optimized process, wafer level void free electroplating is achieved on 300mm wafer.

Acknowledgements

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