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Thermal mechanical behavior of TSVs with WN/Ni as barrier/seed layer system for 2.5D integration

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Abstract

Through silicon vias (TSVs) are regarded as one of the key enabling components to achieve next generation system integration. Many efforts in recent years have paid on new TSV barrier/seed layer schemes to improve step coverage and lower down overall TSV fabrication cost. In this paper, we report on the thermal mechanical assessment of Cu "pumping" (i.e. protrusion) of TSVs with WN/Ni treated at different annealing conditions. Moreover, the impact of different barrier/seed layer systems on the TSV pumping behavior is also investigated. The thermo-mechanical behavior under different annealing temperatures of TSVs having a diameter of 10 µm and a depth of 100 µm has been evaluated by white light optical profiler inspection. The protrusion can be reduced and stabilized when annealed at the higher temperature. Therefore, higher annealing temperature than processing temperature is recommended. Compared to PVD Ti/Cu system, WN/Ni, as TSV barrier/seed layer, tends to have higher Cu protrusions.

1. Introduction

Through silicon vias (TSVs) are regarded as a key enabling technology for the realization of highly miniaturized and complex next-generation systems, as TSV helps in significantly reducing wiring lengths, interconnection latency, and power dissipation. Filling of high aspect ratio TSVs is mainly by means of electro-chemical deposition (ECD) Cu due to its optimal electrical properties, ease of processing and lower cost. However, the coefficient of thermal expansion (CTE) of Cu is much higher (16.7 ppm/°C) than that of Si (2.3 ppm/°C). Therefore, the CTE mismatch between ECD Cu and Si substrate can induce thermal stresses, which may lead to TSV protrusion and interfacial delamination [2-5]. When the ECD Cu is subjected to repeated thermal loadings during the subsequent fabrication process, for instance redistribution layer (RDL), bumping, temporary bonding, die-stacking processes, the induced thermal stress can be accumulated and then result in fatal reliability problems. One way to release the stress and TSV pumping is by annealing. In fact, the TSV wafers could be annealed right after the copper plating process, or after the chemical mechanical polish (CMP) process, or both. To lower down the cost and minimize the CMP steps is one of the concerns from industry.

Physical vapor deposition (PVD) is the most frequently utilized method for barrier/seed layer deposition. However, PVD still suffers some limitations, for instance poor step coverage, overhang, costly and less extendable. Pulsed nucleation layer technology is capable of depositing highly conformal WN films with excellent adhesion and dielectric properties. This paper reports our latest results on fabricating TSV with WN/Ni as barrier/seed layer and the thermal mechanical evaluation of the newly achieved TSV structure.

2. TSV fabrication

The TSV fabrication process are as follows: (a) the TSV fabrication process starts with a 300mm diameter and double-side polished Si wafer. (b) the vias are etched using deep reactive ion etch (DRIE) with the vias having 10 µm in diameter and 100 µm in depth, respectively. (c) after the steps of photoresist stripping and via residue cleaning, a layer of 400nm thick silicon dioxide (SiO_2) is deposited by atom layer deposition (ALD). (d) a 20nm WN/W layer is deposited by pulsed nucleation layer deposition as adhesion layer. (e) a 100nm Ni is deposited by electroless plating as barrier/seed layer. (f) the via conductor is copper, which is deposited by electroplating. The wafer was then examined by X-ray microscopy, which reveals the void free filling of TSVs. (g) The wafers are annealed in an N2 furnace at 200 °C, 350 °C, 450 °C, 600 °C, for 30 minutes, respectively. (g) the Cu overburden layer and barrier/seed layer are removed by CMP, respectively.

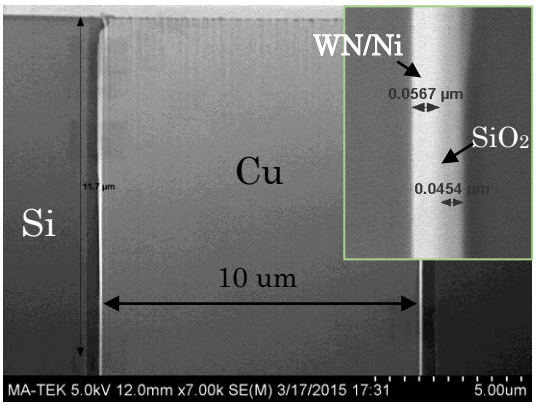

Fig. 1 FIB cross section of TSV with WN/Ni for barrier/seed layer system

3. Results and discussion

After CMP, the wafers are diced into 5×5cm samples and then tested at 200°C for 60 minutes, and 250 °C, 300 °C, 350 °C, 400 °C, 420 °C for 30 minutes, respectively. The Cu protrusion is measured by white light optical profiler. Initial protrusion (or dishing) at room temperature is due to the deviation of planarization in the CMP process. For ease of comparison, the initial height (or dishing) is set as zero, while protrusion height at other temperatures is the measured height subtracts the initial height. Figure 2 compares the Cu protrusion of the annealed TSVs as a function of test temperature. When the TSVs being annealed at 200°C, they show large protrusion at 200°C, and then decrease the protrusion at 250°C. The protrusion increases when tested at 300°C, and drops at 350°C. From 350°C to 420°C, the protrusion increases with test temperature, and the highest protrusion occurs at 420°C. When the annealing temperature is 350°C, the protrusion of TSVs shows similar trend with that of 250°C, but with less protrusion value. When the annealing temperature is 450°C, TSVs show the highest protrusion at 200°C. When the annealing temperature being further increased into 600°C, the Cu protrusion is stabilized with less protrusion level. Compared with different annealing temperatures, TSVs annealed at higher temperatures tends to have less protrusion. Note that there are high Cu protrusion at 200°C. This may be due to the annealing duration is 60 minutes, longer than others.

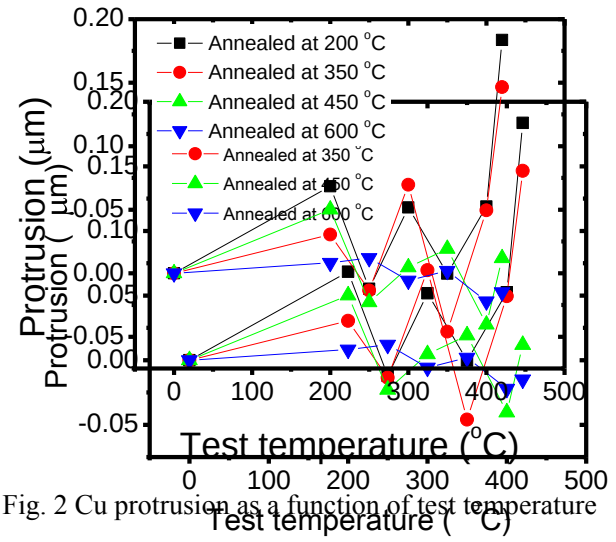

Fig. 2 Cu protrusion as a function of test temperature

PVD Ti/Cu is most widely used material system for TSV barrier/seed layer. For the same TSV geometry and plating chemistry, Figure 3 shows the comparison of Cu protrusion for different barrier/seed systems. When TSVs being annealed at 350°C, the Cu protrusion of Ti/Cu shows different trend to that of WN/Ni. Except 350°C, Ti/Cu shows less Cu protrusion than WN/Ni system. Note the Ti/Cu layer thickness is 100nm/1500nm, which is much thicker than the WN/Ni.

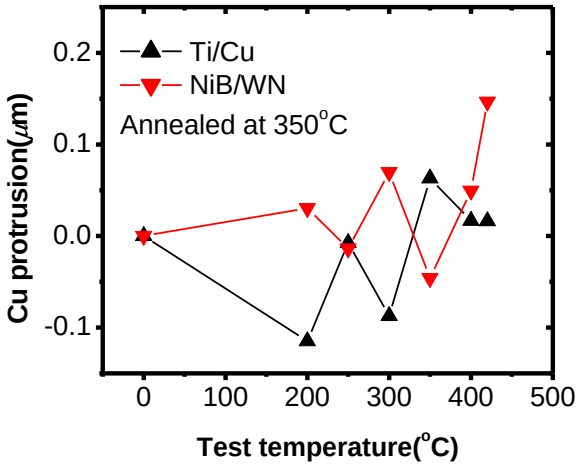

Fig. 3 comparison of Cu protrusion for Ti/Cu and WN/Ni systems.

4. Conclusions

The thermal mechanical assessment of Cu protrusion of TSVs with WN/Ni treated at different annealing conditions is reported in this paper. The TSVs with 10 μm in diameter and 100 μm in depth on the 300-mm silicon wafer are annealed at 200 °C, 350 °C, 450 °C and 600 °C, respectively. According to the Cu protrusion measurement results, the protrusion can be reduced and stabilized when annealed at the higher temperature. Therefore, higher annealing temperature than processing temperature is recommended. Moreover, the impact of different barrier/seed layer systems on the TSV pumping behavior is also investigated. Compared to PVD Ti/Cu system, WN/Ni, as TSV barrier/seed layer, tends to have higher Cu protrusions. And for the industrial usage, to minimize the protrusion not only considering process sequence but also various insulations, barrier/seed and ECD chemistries combinations are still carrying out.

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