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Electroless Nickel Barrier/Seed Layer Deposition on Dielectric Liners for Advanced Cu-TSV Applications

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Abstract

Compared to conventional PVD as a barrier/seed layer deposition technique, electroless plating is used for advanced TSVs such as fine, high aspect ratio (AR), and deep TSVs. In this work, an electroless Ni (EL-Ni) layer is deposited on TSV dielectric liners of SiO_2 by CVD or a polyimide (PI) by vapor deposition. This paper demonstrates great potential of EL-Ni technologies.

1. Introduction

Cu-TSVs with ARs within 10 (ϕ5μm/depth 50μm) can be formed with barrier/seed layers by conventional PVD techniques, as shown in Fig. 1(a). However, the step coverages indicating thickness differences between the top and bottom surfaces of Si deep holes are less than 10%. Low step coverage of barrier and seed layers decreases TSV reliability and yields, respectively. Even when we use an ionized Ti/Cu sputtering system, small voids can be seen from Fig. 1(b) for Cu-TSVs with an AR beyond 12.

To solve this issue, we have proposed EL-Ni that acts as both barrier and seed layers and have previously formed Cu-TSVs (ϕ5μm/depth 50μm/AR 10) with EL-Ni [1]. Ni is well known to be a good barrier film against Cu, and EL plating is a promising candidate to reduce TSV cost. In this paper, we challenge to deposit EL-Ni on SiO_2 TSV liner for 3 types of advanced Cu-TSVs: ϕ2μm/depth 28μm/AR 14, ϕ5μm/depth 85μm/AR 17, and ϕ20μm/depth 200μm/AR 10. In addition, we also attempt to deposit the EL-Ni on a TSV PI liner for Cu-TSVs (ϕ5μm/depth 25μm/AR 5) since the PI liner shows higher step coverage, smaller stress, and lower dielectric constant than standard SiO_2 liners [2].

2. Experimental

Deep Si holes were formed by the Bosch process with SF_6 and C_4F_8. SiO_2 TSV liners were formed by thermal CVD with O_3 and tetraethyl orthosilicate (TEOS). A typical EL-Ni deposition flow is shown in Table I.

3. Results and Discussion

Cu-TSVs (ϕ2μm/depth 28μm/AR 14) are successfully formed with the typical EL-Ni plating conditions that are the same to the previous procedure [1]. As seen from Fig.2, the Cu-TSVs have no failure such as void and seam. The step coverage of the EL-Ni is extremely high as follows: top/top-sidewall/middle-sidewall/bottom-sidewall/bottom, 79/79/68/68/68 nm. The step coverage is around 86%.

EL-Ni can be also deposited on high-AR Si holes (ϕ5μm/depth 85μm/AR 17) under the typical conditions. As seen from the EDX data indicating Ni mapping in Fig.3, the Si holes have a smaller amount of Ni at the bottom than the top. However, the resulting Cu-TSV has no seam although small void is located just 10-15 μm from the via top.

On the other hand, EL-Ni is hardly deposited at the bottom of the deep Si holes with a depth of 200 μm, as seen from Fig. 4(b). Decrease in bath temperature or lowering bath load with paddled agitation is effective to increase the concentration of Ni at the bottom. By optimizing the EL plating conditions, the deep Si holes can be filled with Cu by the subsequent electroplating.

Fig. 5 shows C-t plots that indicate the barrier property of the EL-Ni deposited on a trench MOS capacitor. C_f means final capacitances at the equilibrium state. The C-t plots exhibit little change from the as-depo conditions even after annealing at 400°C, which suggests that the EL-Ni layer has good blocking property against Cu migration.

As shown in Fig.6, a vapor-deposited PI dielectric shows low capacitance, compared to SiO_2 dielectric deposited by plasma CVD at 200°C. Fig. 7 shows cross-sectional SEM images of a Cu-TSV (ϕ5μm/depth 25μm/AR 5) having 800-nm-thick PI liner and 300-nm-thick EL-Ni layers. As seen from this figure, the EL-Ni is conformably deposited with another hydrophilization technique. Consequently, the Cu-TSV is formed without voids, seams, and delamination, which would be expected to be highly reliable TSV formation for high-frequency applications.

Acknowledgements

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References

[1] K.W Lee *et al*. IEEE 3DIC 2014, O13.
[2] T. Fukushima *et al*, *SSDM 2013, p.*866 & SSDM *2014, p.*720.

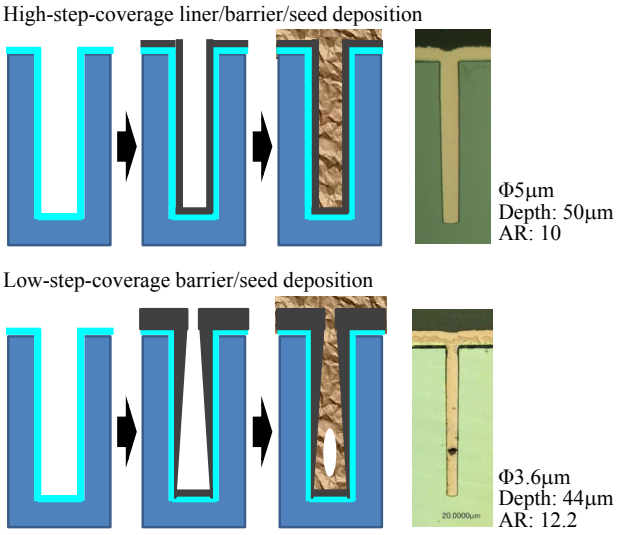

Fig. 1 A serious concern for advanced TSV applications using PVD technology to form barrier/seed layers.

Table I A process flow of EL-Ni deposition for conformal barrier/seed layer formation on SiO_2 TSV liners.

No.	Steps	Temperature
①	Hydrophilization	R.T.-80℃
②	Degreasing	45°C
③	Micro etching	RT
④	Surface conditioning	RT
⑤	Catalyzing	RT
⑥	Activating	RT
⑦	Electroless Ni plating	70℃

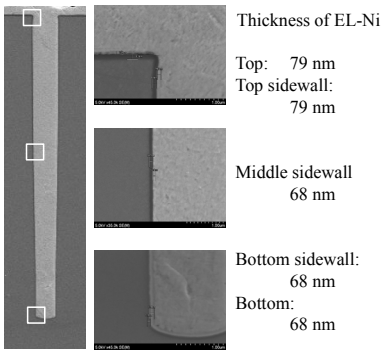

Fig. 2 Cu-TSV formation with an EL-Ni seed layer for fine TSVs (ϕ2μm/depth 28μm/AR 14).

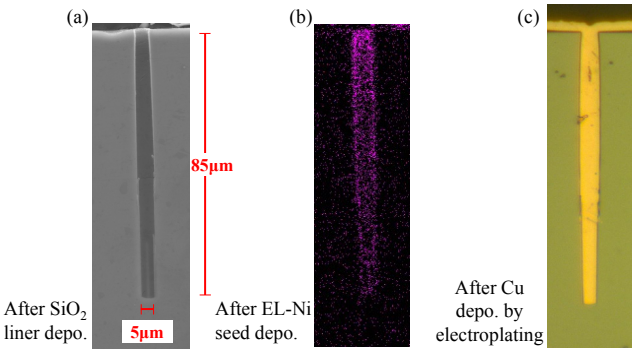

Fig. 3 Cu-TSV formation with an EL-Ni seed layer for high-aspect-ratio TSVs (ϕ5μm/depth 85μm/AR 17).

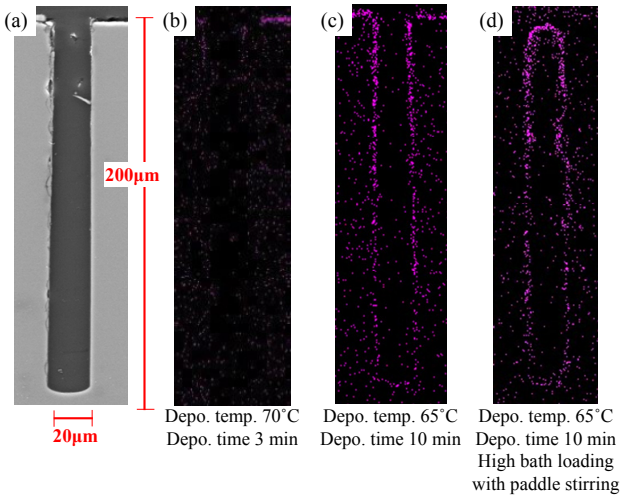

Fig. 4. EL-Ni seed layer deposition for deep TSVs (ϕ20μm/depth 200μm/AR 10).

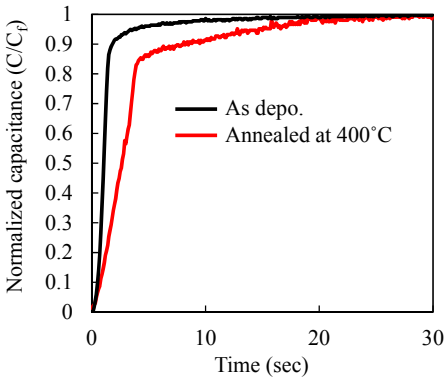

Fig. 5. C-t plots of a trench MOS capacitor composed of Cu-TSVs with an EL-Ni seed layer before/after annealed at 400°C.

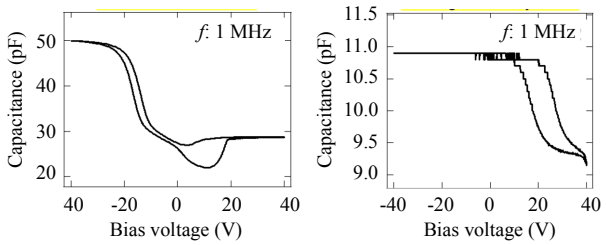

Fig. 6 C-V curves of MOS capacitors with a dielectric layer: SiO_2 by plasma CVD (left) and PI by vapor deposition (right).

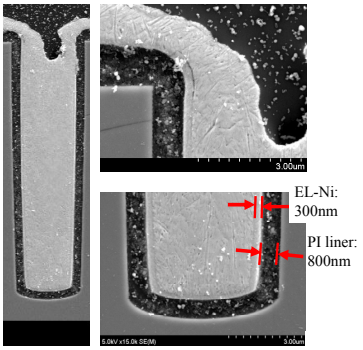

Fig.7. Cu-TSV formation with an EL-Ni seed layer on PI dielectric liner (ϕ5μm/depth 25μm/AR 5).