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A Novel Low Temperature (<500°C) and Low-κ (3.8) Boron Nitride PECVD Offset Spacer Featuring 3D VLSI Integration

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Abstract

In this paper, a novel conformal boron nitride film deposited by PECVD is presented. In view of its low deposition temperature (T_{dep}=480°C), low dielectric constant (κ=3.8) and low wet etch rates in standard clean chemistries, this film is very attractive for the replacement of conventional silicon nitride as offset spacer in 3D VLSI CoolCube™ integration.

1. Introduction

3D VLSI CoolCube™ integration is based on stacked layers of devices fabricated sequentially on top of each other, allowing very high 3D via density and gains in power and performance [1]. However, one of the challenges is the processing of top level devices without degrading bottom ones. Thus, the limited thermal budget allowed for the top transistor fabrication is around 500°C for couple of hours [2]. One of the critical steps in a standard planar Fully-Depleted SOI (FDSOI) MOSFET fabrication is the formation of offset spacers in order to isolate the gate stack from raised sources and drains (Fig. 1).

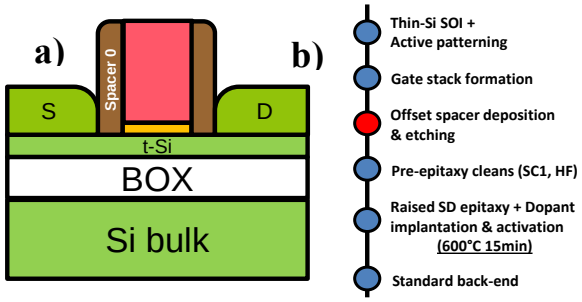

Fig. 1: a) MOSFET on planar FDSOI after raised source/drain epitaxy step; b) Simplified process flow

Actual point of reference (POR) for offset spacer material is silicon nitride (SiN_x) deposited above 600°C by Atomic Layer Deposition (ALD). Attempts to lower the deposition temperature down to 500°C using the same process led to strong degradation of the film during integration. Fig. 2 shows SEM top view pictures of 500°C ALD SiN_x spacer after etch. Holes arose after plasma etching, which is detrimental for the transistor functionality, while wet etch rate in HF increased by a factor two, increasing the consumption of the offset spacer during the pre-epitaxy cleans. Therefore, it becomes necessary to investigate new materials which not only fit with the limited thermal budget constraint, but also meet several integration requirements: (i) CMOS front-end-of-line compatibility, (ii) conformity and uniformity of the film, (iii) integrability and (iv) stability in temperature.

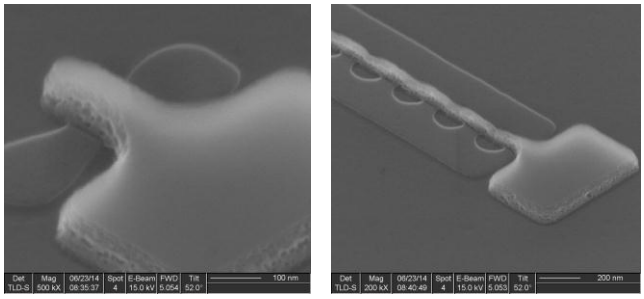

Fig. 2: SEM pictures of 500°C ALD SiN_x after plasma etching

Integration of low-κ dielectrics (SiBCN, SiCOH) to replace silicon nitride has already been demonstrated with gain in ring oscillators speed thanks to reduced parasitic capacitance [3,4]. In this paper, a novel boron nitride (BN) film deposited at 480°C by Plasma Enhanced CVD (PECVD) is presented. Morphological characterization and physical/chemical properties of the film show that PECVD BN film highlights very good characteristics in order to replace conventional SiNx for the low temperature CoolCube™ integration.

2. Material characterization

100nm boron nitride low-κ film was deposited at 480°C on 300mm blanket wafers by PECVD. Material characterization includes ellipsometry for thickness and refractive index (RI) measurement, X-Ray Reflectometry for density and stress extraction using Stoney method. In addition, capacitance and intensity-voltage measurements using mercury probes were performed to evaluate dielectric constant, film leakage at 1MV/cm and breakdown voltage. Table I summarizes the results obtained for as-deposited films and after a 600°C/15min anneal corresponding to the actual thermal budget (TB) of subsequent epitaxy and dopant activation steps [5]. These two steps temperature will be targeted to below 500°C for future 3D sequential devices integration.

Table I: Properties of as-deposited/annealed BN film

	BN as-deposited	BN + anneal
Dep. Temp.	480°C	/
Dep. rate	1.8 nm/min	/
Thickness (nm)	100	100 (0%)
RI@633nm	1.91	1.91 (0%)
Stress (MPa)	-145	-145 (0%)
Density (g/cm^3)	1.78	1.78 (0%)
κ-value	3.8	4.2
Leakage (A/cm²)	1x10^{-7}	2x10^{-7}
Vbd (MV/cm)	5.6	5.4
Composition	B (48%), N (36%), H (11%), other (5%)	B (47%), N (37%), H (11%), other (5%)

No or few variation in physical properties of BN films is found after the 600°C/15min annealing reflecting the good film stability against thermal budgets. Dielectric constant of BN film is greatly reduced compared to SiN_x POR one (κ~6.5-7) and only a slight increase is found after annealing. Current leakage and voltage breakdown on as-deposited film are also slightly degraded after annealing. Nevertheless, further electrical characterization after full integration of the film is needed to conclude.

BN film structure was analyzed using transmission Fourier Transform Infrared spectroscopy in normal incidence for chemical bondings and X-Ray Diffraction for crystallinity of the film (Fig. 3).

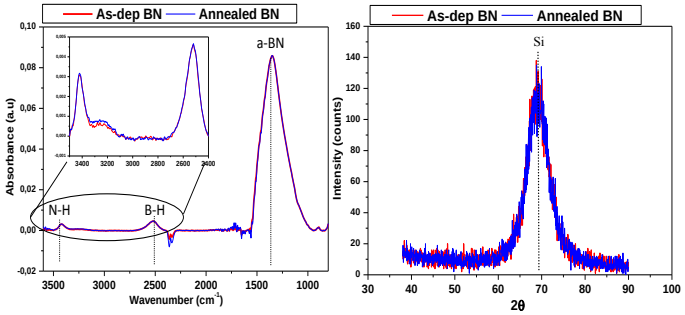

Fig. 3: Transmission FTIR (left) and XRD (right) spectra for as-deposited and annealed (600°C/15min) BN film.

FTIR peak at ~1400cm^{-1} may be related to either hexagonal or amorphous BN [6]. However, XRD measurements show only one peak corresponding to bulk silicon. Hence, as-deposited BN film is amorphous and does not recrystallize upon annealing. In addition, very little change in bond structure is found after annealing, which is confirmed by the unmodified film atomic composition given in Table I and measured using Nuclear Reaction Analysis for boron and nitrogen and Elastic Recoil Detection Analysis for hydrogen. In particular, few hydrogen outgassing occurs during annealing as peaks related to B-H (~2550cm^{-1}) and N-H (~3400cm^{-1}) does not vary. Therefore, in view of material characterizations, we expect that BN film will be stable during epitaxy and dopant activation thermal annealing.

3. Integrability study

After film deposition, the offset spacer formation is done by RIE technique using a two steps plasma process (main etch and over etch). Standard spacer RIE process yields slightly lower dry etching rate for BN than for POR material (-7%) with an over etch selectivity against silicon over 50, resulting in low consumption of the very thin Si channel layer. In addition, spacer should have low wet etch rates (WER) in standard clean chemistries. In particular, ammonia/H_2O_2 mixture (SC1) and HF are used after spacer etching to remove organic residues and native oxide before epitaxy of raised sources and drains. Low WER in SC1 at 60°C, HF (2%) and HF (0.5%)/HCl (1%) at room temperature were measured at 1.5, 0.6 and 1.5 Å/min respectively, ensuring spacer integrity and preventing poly-Si growth on the gate flanks during the epitaxy step.

Finally, 13nm BN film was deposited on patterned structures. The TEM picture (Fig. 4a) highlights excellent step coverage over 95% with a standard deviation of 3.5% for thickness (Fig. 4b).

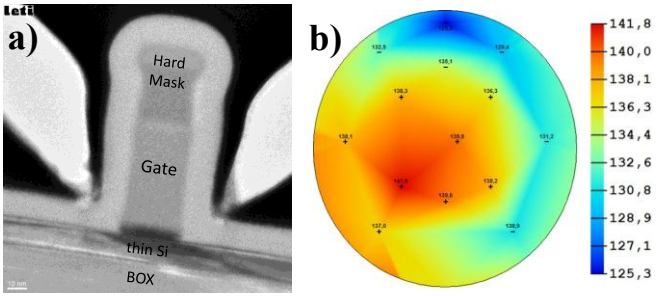

Fig. 4: a) TEM picture after BN deposition; b) thickness uniformity measured by ellipsometry.

4. Conclusions

A novel very conformal BN material deposited by PECVD below 500°C fitting the full 3D VLSI CoolCube™ integration requirement was presented. Thanks to its low temperature process and low permittivity of 3.8 allowing reduction of parasitic capacitances, 3D VLSI CMOS devices performances can be improved. Moreover, thermal stability up to 600°C, RIE selectivity and low wet etch rates in standard clean chemistries should ensure the offset spacer integrity throughout the full integration.

Acknowledgements

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