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Local Stress Effect due to Operation-Heating-Induced Adhesive Expansion on Transistor Performances in 3D IC

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Abstract

A three-dimensional stacked IC (3D IC) consists of several materials such as Si substrate, metal for TSV and microbump, organic adhesive, and so on. These materials generate coefficient of thermal expansion (CTE) mismatch. On the other hands, operating circuits generate heat in Si substrate. Both the CTE mismatch and heat generation during circuit operation induce local stress by expansion of organic adhesive injected around metal microbumps. This paper reports analysis results of effects of adhesive expansion on transistor performances using finite element method (FEM) simulation and transistor characteristics measurement.

1. Introduction

A three-dimensional stacked IC (3D IC) is a one of promising method for enhancement of electron-device performances [1]. However, great anxiety in electrical and mechanical reliability issues are increasing among 3D IC researches for production of 3D IC [2]-[5]. Conventional 3D ICs consist of vertically stacked several thin IC chips with lots of through Si vias (TSVs) and metal microbumps that electrically connect each IC chips. Metal microbumps are surrounded by organic adhesive called underfill material. In general, coefficient of thermal expansion (CTE) of the underfill material is larger than that of metal microbumps. On the other hand, a circuit operation generates heat in IC chip. Such as processor chip sometimes reaches high temperature more than 80°C by circuit operation [6]. As shown in Fig. 1, CTE mismatch and circuit-operation heat induces local bending stress in thinned Si chip by large expansion of underfill. The local stress would affect transistor performance in thinned Si chips. However, the effect of this local bending stress haven't been investigated enough. Therefore we should evaluate the effect of the local bending stress on transistor characteristics for realization of high performance 3D IC.

In this paper, we have calculated the local stress caused by adhesive expansion using finite element method (FEM) simulation, and evaluated the effect of the local stress induced by the combination between CTE mismatch and heat on transistor characteristics using the test structure.

2. Experiment

Figure 2 shows a simulated structure to calculate the local stress induced by adhesive expansion. The model was composed of thin Si chip, 25 metal microbumps, underfill material, and Si substrate. Thin Si chip was stacked on metal microbumps and underfill formed on Si substrate. Si chip thickness was 30 um, microbump size and height were 20 by 20 μm and 20 μm. In this simulation, the material of microbumps was Cu. Table 1 shows physicality values of each material for simulation. A glass transition temperature (T_g) of underfill material was 75°C. The stress and strain was calculated at temperature changed to 50°C from 23°C.

Figurer 3 shows a schematic cross-section of test structure to evaluate the effects of local bending stress. The test structure is composed of Si (dummy) microbumps, an organic adhesive, and a thinned Si chip stacked on Si substrate. This test structure can evaluate only local bending stress due to the circuit-operation heat and the CTE mismatch between organic adhesive and Si microbumps. The test structure was fabricated with following processes, as shown in Fig.4. First, Si microbumps were formed on the Si substrate by inductively coupled plasma reactive ion etching (ICP-RIE). The bump size and height were 20 μm by 20 μm and 20 μm. The bump pitches was 50 μm. Then, the thinned Si chips were bonded on the Si substrate which was coated with an adhesive A. In this paper, the thinned chip thickness was 30 μm. After that, underfill material was additionally coated around the thinned chips depicted as the adhesive B in Fig. 3. The chip and the Si substrate were temporarily exposed in vacuum atmosphere and opened to the air to completely fill gaps between the thinned chip and the substrates by the epoxy. Finally, the underfill material was cured at 180°C for 30 min. After fabrication of the test structure, we measured the I-V characteristics of transistor fabricated on the thin IC chip at temperature of 23°C and 50°C.

3. Results and discussion

Figure 5 shows cross sectional image of simulation result across the center of a microbump. Here, the image shows the normal stress on X direction. We can observe the compressive stress distribution on top surface of Si chip and both tensile and compressive stress on bottom surface of Si chip. This simulation result indicates that CTE mismatch and circuit-operation heat induce large performance dispersion of transistor fabricated on Si chip surface.

Figure 6 shows change ratio of drain current due to temperature change. We measured pMOSFETs (p-type Metal Oxide Semiconductor Field Effect Transistors) at temperature of 23°C and 50°C. Here, gate voltage, source voltage, and body bias were 1.8 V, 0V, and 0 V. Gate width was 10 μm, and gate lengths were 2 μm and 20 μm. And we measured both test structure with and without Si microbumps to evaluate the effect of CTE mismatch. The pMOSFETs were located at several points on thinned IC chip. In the case of the test structure without Si microbumps, there was little change ratio difference between measured transistors. In contrast, there was large dispersion of change ratio when the test structure had Si microbumps. These results clearly shows that the large

dispersion of drain current change ratio was induced by CTE mismatch between underfill material and microbumps.

4. Conclusion

We have investigated the effects of local bending stress caused by thermal expansion of organic adhesive in detail with simulation and test structure simulated actual 3D IC. Simulation results indicated stress distribution on thinned Si chip. In addition, the large dispersion about drain current change was obtained when the test structure has Si microbumps. These results indicated that the combination of CTE mismatch and heat induced large dispersion of transistor performance change due to circuit-operation heat. In order to realize higher performance 3D IC with transistor performance degradation and fluctuation, careful design including layout of microbumps and transistors is strongly required.

Acknowledgments

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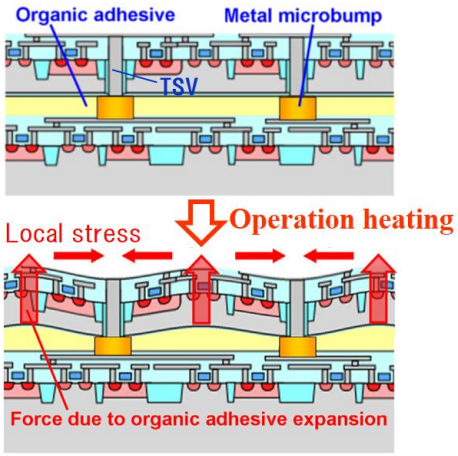

Fig. 1. Schematic cross-section of 3D IC expressing local stress due to adhesive expansion induced by heat generation in circuit operation and the CTE mismatch between organic adhesive and metal microbumps.

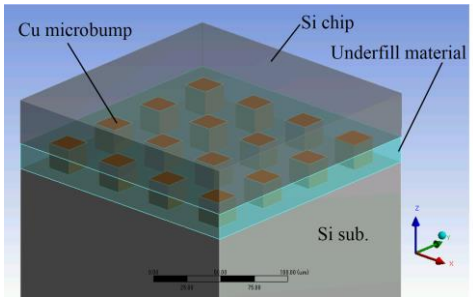

Fig. 2. Simulation model for analysis of local bending stress induced by the CTE mismatch and heat generation.

Table 1. Material constant.

Material	Young's modulaus (GPa)	Poisson's ratio	CTE (10^{-6}/K)
Si	166	0.07	3
Cu	129	0.34	17
Organic adhesive	1.9	0.37	89 (Below Tg) 139 (Above Tg)

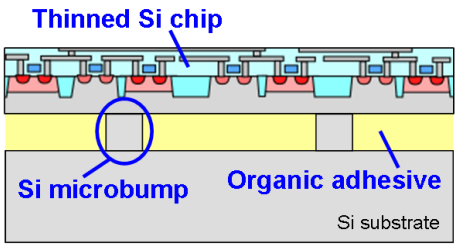

Fig. 3. Schematic drawing of the test structure to evaluate the effect of local bending stress due to organic adhesive expansion.

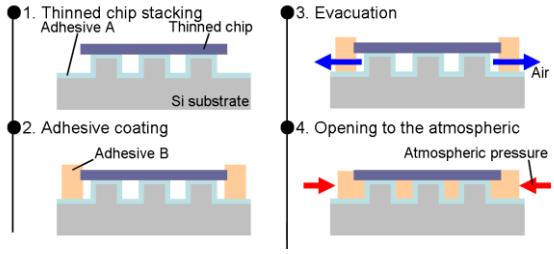

Fig. 4. Process flow of the test structure with Si microbumps.

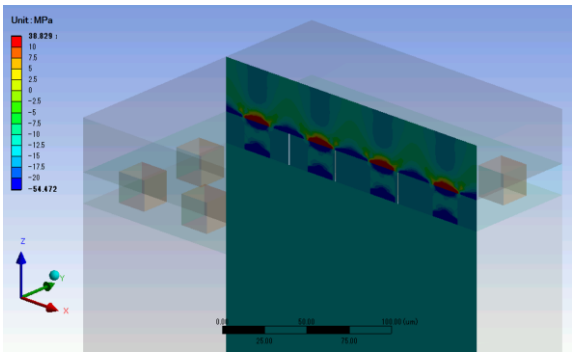

Fig. 5. Simulation result of normal stress on X direction at temperature changed from 23°C to 50°C.

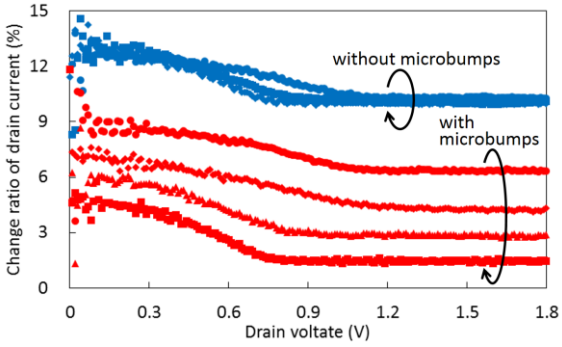

Fig. 6. Effect of local bending stress on drain current of pMOSFET fabricated in thin IC chip from 23°C to 50°C with and without Si microbumps.