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Capacitance Characteristics of Low-k Low-Cost CVD Grown Polyimide Liner for High-Density Cu-TSVs in 3D-LSI

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Abstract

Minimizing the capacitance arising from Cu-TSVs has been rigorously considered in order to enhance the 3D-LSI performance. We have systematically investigated the role of chemical vapor deposited (CVD) polyimide (PI) liner in Cu-TSVs in reducing the TSV capacitance. It is confirmed that CVD grown PI greatly helps to reduce the TSV capacitance as compared to the conventional PECVD-SiO_2 liner. At the same time the presence of hysteresis and a large shift along the voltage axis impose reliability concerns, if used the Cu-TSVs with PI liner for the bias voltage above > ±20V. In over all, the large reduction in capacitance along with the conformal deposition of PI in the TSVs having less than 3 μm-width with aspect ratios of greater than 10 reveals the potential application of CVD grown PI in 3D-LSI.

1. Introduction

Through-Si Via (TSVs) is a key enabling technology in 3D-LSI. In 3D-LSI various functional chips are vertically stacked and electrically connected through TSVs in order to reduce the resistive-capacitive delay and to achieve the small form factor, which is extremely difficult to realize in the conventional 2D-LSI. In TSVs, low-temperature grown plasma enhanced chemical vapor deposited (PECVD) SiO_2 is used as dielectric liner. Owing to its high dielectric permittivity along with poor quality and the low step coverage, the development of an alternative liner material has been considered as an important process in 3D-LSI. Organic polyimide is known for long due its good mechanical property and near perfect electrical insulation at harsh environment. Spun on polyimide and BCB as a liner in TSVs were reported in [1] and [2], respectively. However, in order to achieve conformal deposition of PI in high aspect ratio TSVs, spin-coat process might not be viable. Though vapor polymerization of PI is known for long [3], only very recently VDP PI in TSV was reported [4]. *It is highly important to know the capacitance characteristics of dielectric liner used in the signal transmission. In this study, we report the capacitance characteristics of CVD grown PI with different thicknesses in Cu-TSVs, before and after post heat treatment for their use in signal TSVs.*

2. Experimental

After forming TSVs with diameter of 3 μm to 30 μm by conventional Bosch process, conformal growth of PI liner with 85% step coverage was carried out by co-polymerizing the monomers PMDA and ODA at 180 C. The details regarding the TSV filling can be found in elsewhere. [5-7]

3. Results and Discussion

The low modulus of PI has tremendously reduces the thermos-mechanical stress in Si [5] and Cu pop-up in Cu-TSVs [6].This was further confirmed by the μ-XRD [6]. X-section optical images of completely filled Cu-TSVs with PI liner is shown in fig. 1, and the schematic of MPS structure used in this study is shown in fig. 2.

Shown in fig. 3 is the typical C-V curves obtained on M-PI-SC(MPS) structure having 250 nm-thick PI annealed at 200 C for 30 minutes in flowing N_2 atm., and it depicts the C-V curves for 10 continuous measurement cycles at different stress voltages range. Qualitatively, there are two features (i) Upto the stress voltage of ±10 V, we observed less 2 V of hysteresis, which is quite similar to the PECVD grown SiO_2 liner. However, beyond that the magnitude of hysteresis increased with increase in the stress voltage. (ii) Beyond the stress voltage of ±20 V, the flat-band voltage, Vfb, shifts positively along the voltage axis. This reveals the presence of negatively charged traps (mobile/immobile) in PI layer. The amount of hysteresis for each C-V cycle is summarized in fig. 4. The presence of hysteresis and the shift in Vfb is of reliability concern associated with the PI liner in Cu-TSVs when it is deployed in the signal line, since the hysteresis may lead to the signal delay or partial signal loss. As long as the active signal line is stressed below the ±10 V limit, it should not be a problem.

From fig. 6, it is found that annealing of PI up to 300 C helps not only to reduce the C, but also to bring the Vfb close to 0 V. However at 400 C, the C increases along with the positive Vfb shift. It is possibly due to the degradation of PI as observed in TDS studies. [6] The absence of Vfb shift with frequency (fig. 6) reveals that CVD-grown PI is free from mobile impurities or surface state.

In **summary**, the potential application of CVD grown PI as dielectric liner in high-density Cu-TSVs with very large aspect ratios is confirmed. The low-k and low modulus values of PI helps to reduce the TSV capacitance and thermo-mechanical stress in Si induced by Cu-TSVs, respectively. Although the hysteresis and the Vfb shift in C-V curves are of reliability concerns, it is not detrimental in using PI liner in TSV for the bias voltage of ≤ ±20 V.

Acknowledgment

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References [1] E. Beyne *et al*, *IEEE T-CPMT*, 1, 833 (2011). [2] Q. Chen *et al*,*IEEE T-CPMT*, 3, 724 (2013). [3] Y. Takahashi *et al*, *IEE J. Elect. Insul. Mater.*, EIM-85, 49 (1985). [4] B. Sapp *et al*, *IEEE IITC*, pp.1-3 (2012). [5] M. Murugesan *et al*. *IEEE ECTC* pp.636-640 (2014). [6] M. Murugesan *et al*. *IEEE IEDM* pp.374-377 (2014). [7] M. Murugesan *et al*. *IEEE ECTC* sess.2-6 (2015).

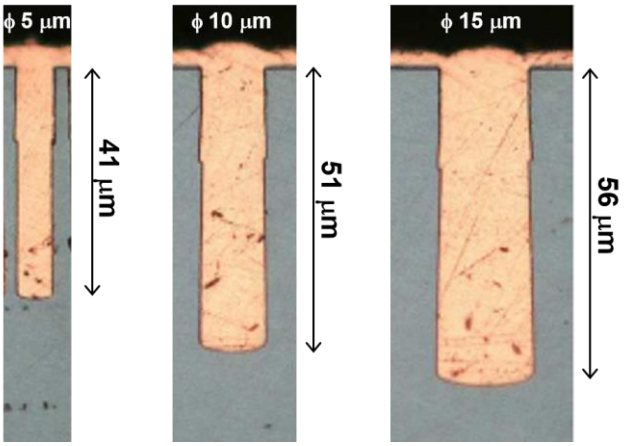

Fig. 1: X-section optical microscopic image revealing the blank Cu-TSV dimensions with CVD polyimide liner.

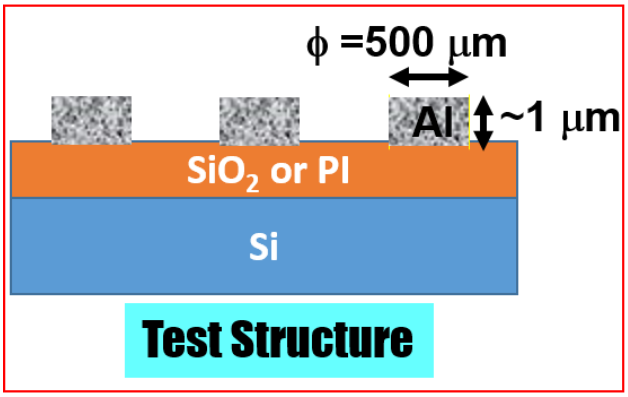

Fig. 2: Test MPS structures used to study the Capacitance-Voltage (C-V) characteristic of PI liner

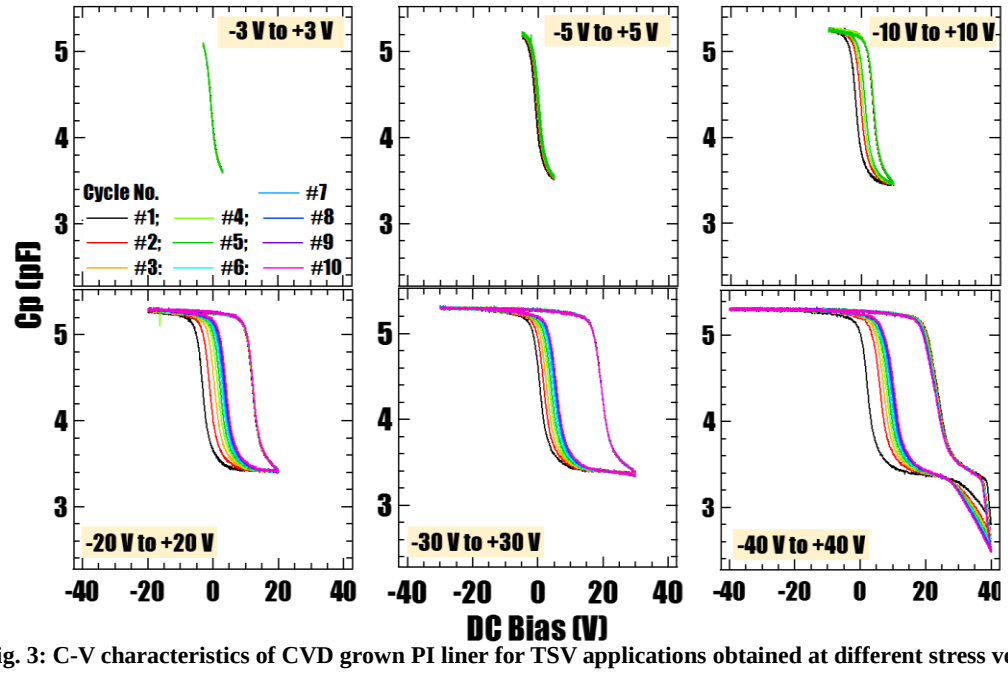

Fig. 3: C-V characteristics of CVD grown PI liner for TSV applications obtained at different stress voltages.

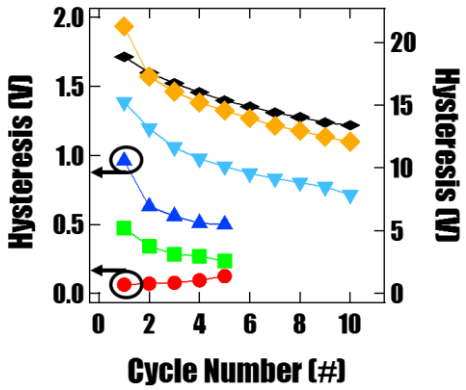

Fig. 4: Plot of hysteresis values against number of C-V cycles.

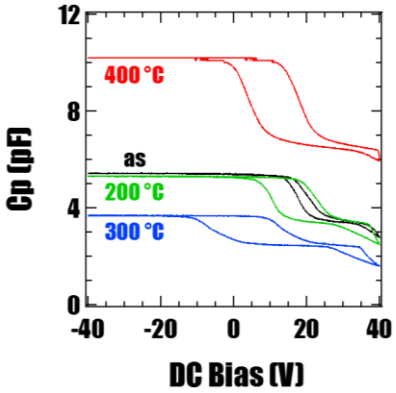

Fig. 5: Effect of annealing of 250 nm-thick PI liner .

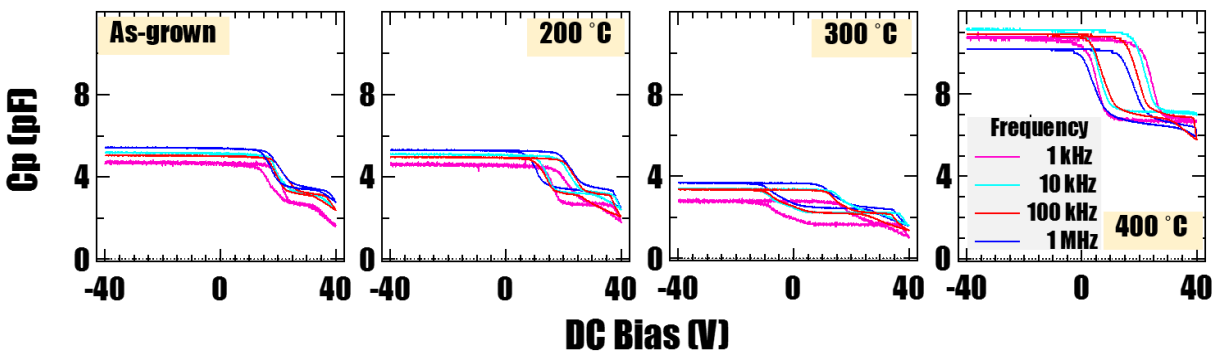

Fig. 6: Frequency dependent C-V characteristics of annealed PI liner at different temperatures.