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Proposal of Tunneling and Diffusion Current Hybrid MOSFET

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Abstract

This paper proposes a novel tunneling and diffusion current hybrid MOSFET. Due to the structural parameter optimization for both tunneling and diffusion carrier transports using device simulation, a 20 mV/decade subthreshold swing and 500 μA/μm current drivability are achieved simultaneously. A process flow for the 3D integration is also provided.

1. Introduction

Low power operation with a sufficient signal processing speed is important characteristic of LSI for next generation mobile and machine to machine (M2M) applications [1]. Tunnel Field Effect Transistor (TFET) [2] has been paid much attention that can operate under a low supply voltage due to its small subthreshold swing factor (S-factor) of less than 60 mV/decade, which is the theoretical minimum value of diffusion current at room temperature. However, compared with diffusion current of thermal carrier emission, drivability of tunneling current is much lower by several orders of magnitude [3]. In this paper, we propose a novel tunneling and diffusion current hybrid MOSFET utilizing both small S-factor of tunneling current and high drivability of diffusion current. The basic working principle and device structural parameter optimization are investigated using device simulation.

2. The Device Concept

Fig.1 shows the cross-sectional view of proposed tunneling and diffusion current hybrid MOSFET. Both n^+ and p^+ parts are used for the source terminal for diffusion and tunneling current respectively. The channel and the drain are commonly used for these two carrier transports. The two current components are controlled by dual gate electrodes (Gate 1 and 2) with the same voltage. Fig.2 shows band diagram of (a) diffusion region and (b) tunneling region respectively. The working principle of this device is to switch dominant current from tunneling current to diffusion current. In the subthreshold region, tunneling current firstly flows with small S-factor of less than 60 mV/decade. Under the on-state the diffusion current overtakes the saturated tunneling current to reach several 100 μA/μm.

3. Optimization of Hybrid MOSFET Structure

Fig.3 shows the simulated I_D-V_G characteristics of the structure shown in Fig.1. Here, the BBT nonlocal model of TCAD Atlas by SILVACO was utilized for device simulation in this work to calculate the band to band tunneling current. In Fig.3, diffusion current is larger than tunneling current at the all range of gate voltage, which makes the effect of tunneling current unavailable. Fig.4 shows the modified structure. We adopted a vertical tunneling structure [4] to boost the tunneling emission efficiency. By this structure the electric field intensity is enhanced at the corner of p^+ source by Gate 2. An introduction of n^+ layer (5 nm thickness) between p^+ source and gate insulator film at Gate 2 is for V_{th} adjustment of tunneling current. Diffusion part and tunneling part are separated by this p^+ source extended under the gate, suppressing leakage current caused by accumulation-type or junction-less channel (N_{ch}) between n^+ source. Fig.5 shows the simulated I_D-V_G characteristics of modified structure. Tunneling current dominates the total current in subthreshold region. The minimum value of S-factor of 17.7 mV/decade and a relatively high drivability current of 472 μA/μm were obtained by the proposed hybrid MOSFET.

4. Examination of the Effects of Structural Parameters

It is important to adjust each I_D-V_G characteristics of diffusion and tunneling current to obtain both small S-factor and high drivability. Figs.6 and 7 summarize the effects of workfunction of Gate 2 and n^+ region between p^+ source and gate insulator film at Gate 1, respectively. The diffusion current can be tuned by the workfunction of Gate 1, and tunneling current can be tuned by either concentration of N_{n+} or thickness of T_{n+} as well as workfunction of Gate 2 as shown in Fig.6 and 7. Fig.8 (a) and Fig.8 (b) show three types of leakage current of various sets of L_1/L_2 defined in Fig.4. The first leakage component is the diffusion leakage which flows from n^+ source through accumulation channel (L_1/L_2 = 80/30 nm). This leakage depends on L_1 and increases when $L_1 \geq 80$ nm, the overlap length (L_G - L_1) is ≤ 20 nm. The second component is the tunneling leakage from p^+ source to n^+ layer (L_1/L_2 = 50/20 nm). This leakage is caused by n^+ layer which is not fully depleted by p^+ source. The third component is tunneling leakage that flows directly from p^+ source to n^+ drain (L_1/L_2 = 25/15 nm). This leakage is caused by punch-through of p^+ source and n^+ drain when $L_1 < 30$ nm at V_{DS} = 1.0 V. These leakage current often results in increasing the S-factor. Therefore L_1/L_2 must be optimized to minimize these leakage components. Fig.9 shows I_D-V_G characteristics of the condition that the gate length is scaled down to 50 nm. L_G, L_1 and L_2 are reduced by half respectively, and V_{DS} is also decreased to 0.5 V. The effect of horizontal tunneling leakage caused by halved L_1/L_2 is sufficiently suppressed. The obtained minimum value of S-factor was 21.4 mV/decade. This result implies the proposed hybrid MOSFET is scalable with supply voltage scaling. Fig.10 shows minimum value of S-factor versus on-current drivability for various structural parameters. The result with center parameters in Fig.4 is plotted at the lower left, having the smallest value of S-factor.

Furthermore, Fig.12 shows 3D structure of tunneling and diffusion current hybrid MOSFET and its proposed process flow. The tunneling current side channel and diffusion current top channel are integrated by the use self-aligned processes.

5. Conclusion

The novel tunneling and diffusion current hybrid MOSFET was proposed and optimum structure simulated current-voltage characteristics are demonstrated. A 20 mV/decade minimum S-factor and 500 μA/μm current drivability are obtained simultaneously.

References

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[2] W.M.Reddik et al., Proc.IEEE. (1995) 490.
[3]A.C. Seabaugh, Proc. IEEE. 98 (2010) 2097.
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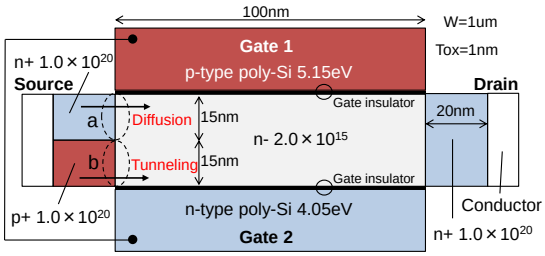


Fig.1 Concept viewgraph of tunneling and diffusion current hybrid MOSFET.

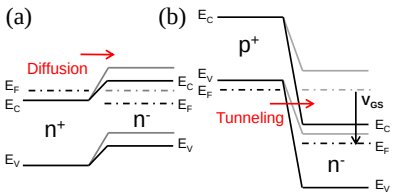


Fig.2 Band diagram of (a) diffusion region and (b) tunneling region

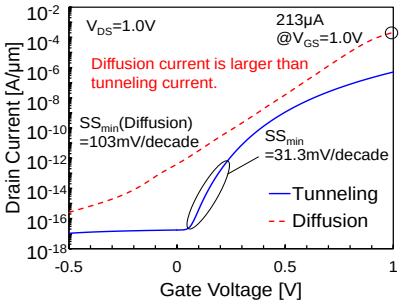


Fig.3 I_D-V_G characteristics of Fig.1 structure. Diffusion current is larger than tunneling current at the all range of gate voltage.

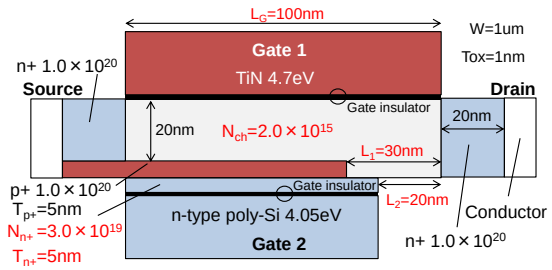


Fig.4 Modified structure of Hybrid MOSFET. Each parameter is adjusted so that tunneling current is larger than diffusion current in subthreshold region and S-factor of diffusion current is minimized.

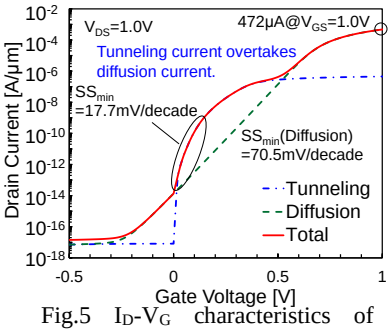


Fig.5 I_D-V_G characteristics of modified structure. Small S-factor and high drivability are obtained.

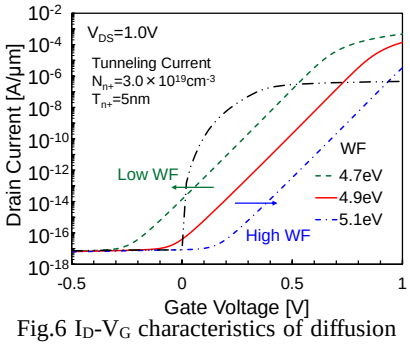


Fig.6 I_D-V_G characteristics of diffusion current can be shifted by work function (WF) of Gate 1.

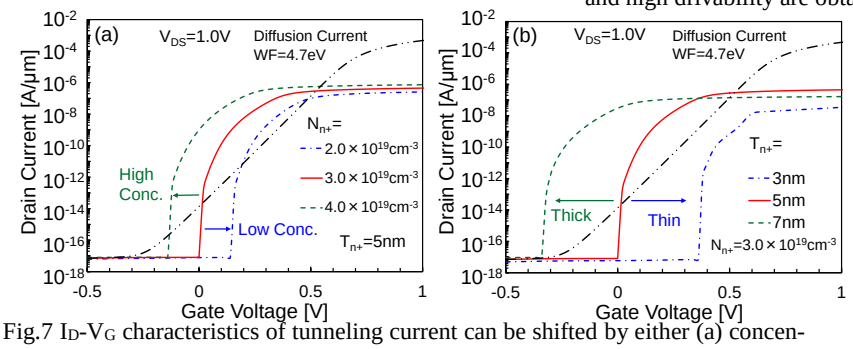


Fig.7 I_D-V_G characteristics of tunneling current can be shifted by either (a) concentration or (b) thickness of n^+ region between p^+ source and gate insulator of Gate 2.

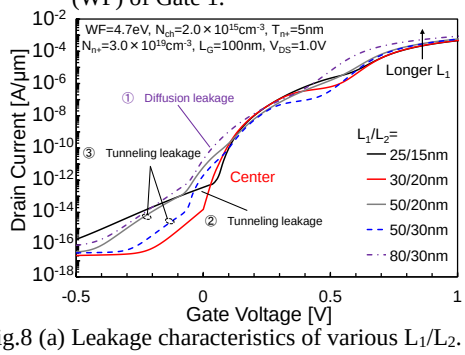
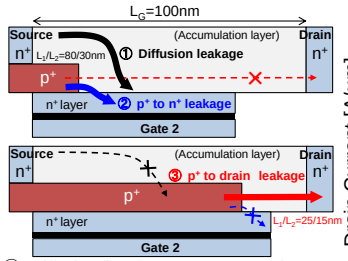


Fig.8 (a) Leakage characteristics of various L_1/L_2.



① Diffusion flow from n+source to n+layer through accumulation channel where $L_1 \geqq 80$ nm

② Tunneling flow from p+source to n+layer where $L_1 - L_2 \geqq 30$ nm

③ Tunneling flow from p+source to n+drain where $L_1 < 30$ nm

Fig.8 (b) Schematic diagram of each leakage path

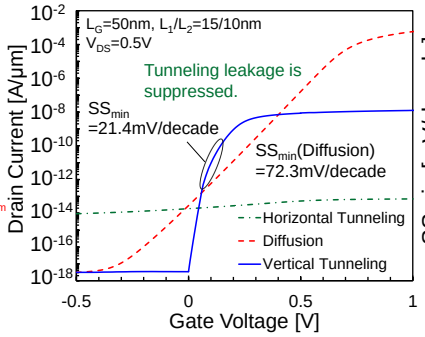


Fig.9 I_D-V_G characteristics of hybrid MOSFET with 50 nm gate length.

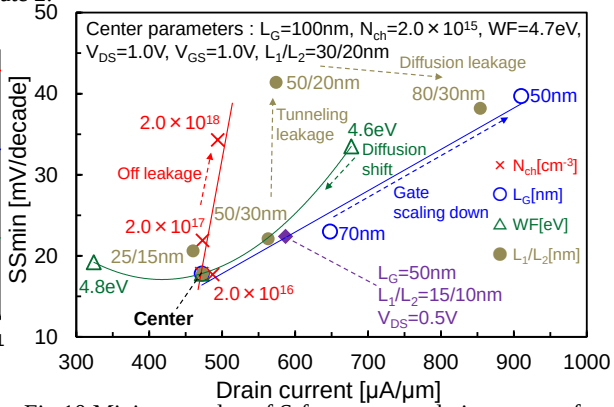
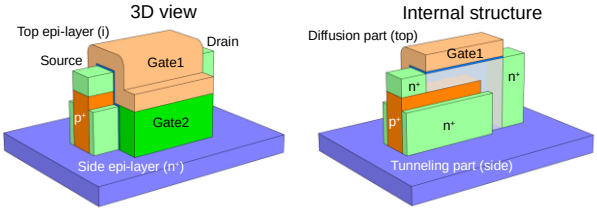


Fig.10 Minimum value of S-factor versus drain current of various parameters. Plot ◆ is the data of Fig.9.



- Fin formation with hard mask on SOI
- SiO_2 deposition (for p^+ I/I mask)
- SiO_2 patterning
- p^+ ion implantation
- SiO_2 etch-back (~10nm)
- n^+ epitaxial growth (side 5nm)
- Silicon (epi-layer) dry etching (~30nm)
- Hard mask and SiO_2 removal
- SiO_2 deposition
- SiO_2 side wall etching
- Intrinsic epitaxial growth (top 20nm)
- SiO_2 removal (side wall)
- Gate oxidation
- Gate electrode formation
- S/D formation
- Contact metallization

Fig.11 (a) 3D structure of Hybrid MOSFET (b) Proposed process flow to fabricate 3D Hybrid MOSFET