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Trap-Assisted Tunneling Effects on Gate-Induced Drain Leakage in Silicon-Germanium Channel pFET

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Abstract

The use of Silicon-Germanium as a channel material in high-k metal gate first pFET technologies of 32nm and beyond has been widely accepted for high performance and low power applications. However, gate-induced drain leakage components and mechanisms are dominant compared to all the other leakage mechanisms in high threshold voltage devices. This work analyzes the effect of trap-assisted tunneling on GIDL using atomistic Monte-Carlo simulations and experimental data and highlights its importance for scaled supply voltages in SiGe channel pFET.

1. Introduction

Silicon-Germanium (SiGe) is an important channel material that serves a replacement to silicon channel because of its higher mobility and lower threshold voltage which makes it suitable for high performance and low power applications [1]. However, gate-induced drain leakage (GIDL) was the dominant leakage component in high threshold voltage (HVT) pFET devices due to reduced bandgap [2]. The increasing use of TCAD to predict the behavior by optimization of physical models and their parameters is useful for capturing this dominance of GIDL, particularly for HVT device designs.

In this work, a comprehensive analysis of trap-assisted tunneling (TAT) at the sidewall junction as one of the GIDL mechanisms in 30nm SiGe channel pFET is presented by first simulating the dopant profiles using a Monte Carlo simulator of a TCAD tool which takes into account the presence of germanium and related effects [3]. The results obtained by device simulation of accurately extracted dopant profiles and calibrated process parameters are compared with experimental data to analyze and validate the TAT effects on GIDL for different bias conditions.

2. Experiment and Simulations

A standard state of the art 32nm high-k metal gate technology with SiGe channel thickness of 10nm and concentration of 30% with a thermal budget of around 1000^{o} C is used in this work for pFETs [4][5]. The process flow is similar to Si channel with the exception of an additional SiGe epitaxial layer step. GIDL measurements are taken according to the setup described in [3], compared with calibrated process flow and the electrical characteristics with short channel behavior is shown in Fig. 1. It can be seen that the measured $I_D - V_G$ characteristics, saturation threshold voltage (V_{TSAT}) and DIBL roll-off matches with the device simulation. The simulation deck can now be used to analyze the TAT effects on GIDL in OFF state $(V_G = 0V)$ for different V_D.

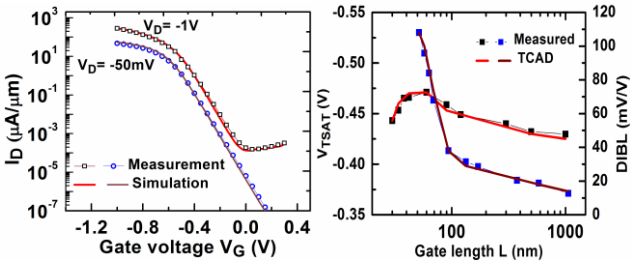


Fig. 1. (a) $I_D - V_G$ characteristics of 30nm SiGe channel pFET in linear and saturation region. (b) V_{TSAT} and DIBL roll off comparison of experiments and simulations.

The GIDL is mostly either due TAT at the drain extension and sidewall or/and band to band tunneling (BTBT) at the drain surface and sidewall region. Each of these mechanisms dominate under specific bias voltages. This paper highlights the contribution of sidewall TAT component as one of the important GIDL mechanisms and its dependence on bias voltages of drain and gate. As bandgap is one of the most important parameter in GIDL calculations, the SiGe bandgap is accurately determined using nearest-neighbor

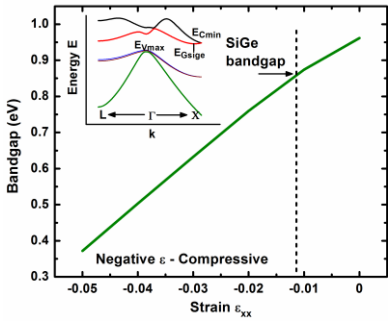
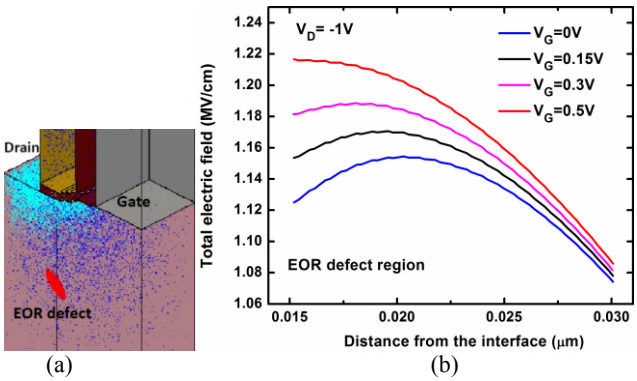


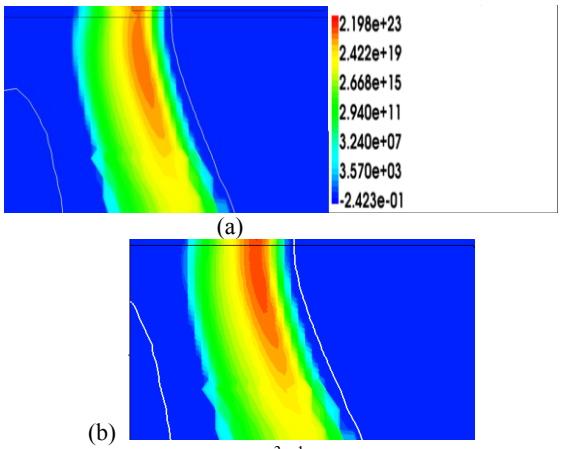
Fig.2 SiGe bandgap determination from tight binding method



(a) (b)

Fig. 3. (a) EOR defect (red patch) obtained from 3-D atomistic Monte-Carlo diffusion simulations after RTA step (b) Total E-field profile in the EOR defect region for different gate bias.

$sp^3d^5s^*$ tight-binding method with strain effects within the virtual crystal approximation [6] as shown in the inset of Fig. 2. The variation of compressive hydrostatic strain with bandgap is plotted and accurate bandgap is determined for the strain used in SiGe channel in this work as shown in Fig. 2. An additional doping induced bandgap narrowing is also taken for the range of doping levels used in this work. Fig. 3(a) shows the presence of end of range (EOR) defects formed at the amorphous/crystalline interface sidewall due to the local enhancement of electric field in this region. The pre-halo germanium preamorphization implant (PAI) used to realize a shallow junction depth and to contain the short channel effects leads to this clustering of defects. The EOR defect is located at a distance of around 16nm from the interface and extends up to 23nm. The effect of electric field in the EOR defect region with Ge PAI is evident in Fig. 3(b). It can be seen that the electric field is significant in this region and changes with gate bias. The effect of gate bias decreases after the defect region (beyond 30nm). This region will contribute to an additional GIDL component in addition to GIDL due to BTBT. The profiles and contours of tunneling rate are zoomed in this region of interest and shown in Fig. 4. It can be seen that the total tunneling rate in the defect region is also affected by gate bias, thus



(a)

(b)

Fig. 4. Total tunneling rate ($cm^{-3}s^{-1}$) in the EOR defect region for V_G= 0V (b) V_G= 0.3V.

confirming the effect of increased electric field. The presence of SiGe channel affects the dopant activation, transient enhanced diffusion and the implantation damage of Ge PAI [7]. Therefore, the contribution of TAT from PAI to GIDL in silicon channel is not significant (about an order lower than SiGe channel) whereas it is found to be more in these devices. Fig. 5 shows the effect of varying drain bias on total GIDL and sidewall TAT. The figure clearly shows that the TAT contribution from the defect region to GIDL is more dominant as the supply voltage is decreased. This is

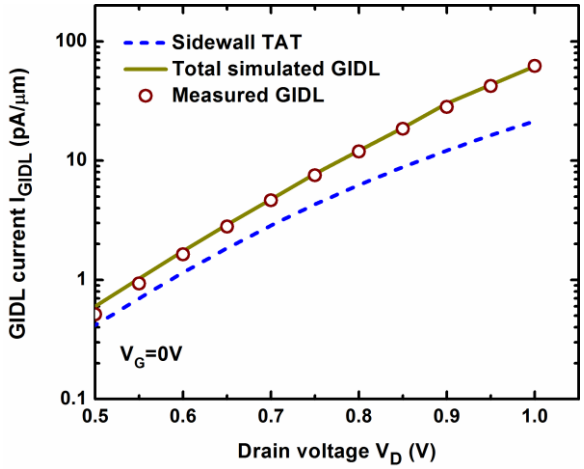


Fig. 5. GIDL variation and sidewall TAT contribution for different values of drain bias.

because the BTBT contribution to GIDL decreases rapidly with decreasing drain voltage. Thus, this component of GIDL will be a major bottleneck for decreasing GIDL in scaled pFET technologies using SiGe channel.

3. Conclusions

The effects of TAT at the sidewall junction region on GIDL in SiGe channel pFET are shown in this work. TAT in OFF-state (V_G= 0V) due to Ge preamorphization implant used before the halo implant becomes relatively more significant for lower supply voltages. Proper optimization of Ge PAI implant and anneal cycles is required to mitigate this effect without compromising with performance.

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