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1/f Noise Performances and Noise Sources of Accumulation Mode Si(100) n-MOSFETs

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Abstract

An improved CMOS technology built upon simultaneously high-speed and low noise MOSFETs has been finally achieved. Not only the drivability of accumulation mode MOSFETs has been improved but their noise level has been also reduced when compared to conventional inversion mode ones, like it has been demonstrated here for the n-MOSFETs.

1. Introduction

The noise of Complementary Metal Oxide Semiconductor (CMOS) is dominated by the 1/f noise. Its level unfortunately increases continually while scaling the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) size and limits the performance of all the electronic devices, especially those for analog and RF applications [1]. The challenge nowadays is to not only provide the society with novel CMOS technologies delivering better reliability and improved electrical performances but also lower noise.

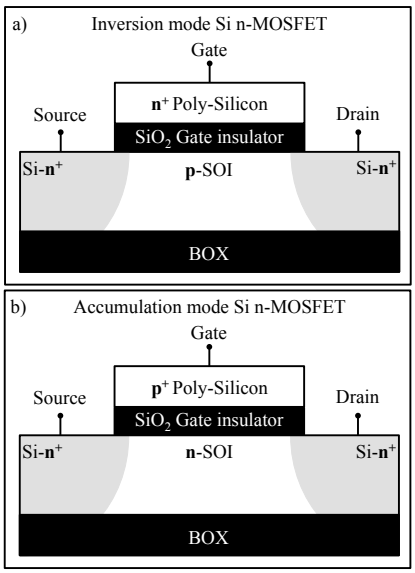

Fig. 1 Schematic of an inversion mode n-MOSFET (a) and of an accumulation mode n-MOSFET.

Among all the possibilities investigated to meet this challenge, a novel CMOS technology based on a newly developed MOSFET working on accumulation mode rather than the conventional inversion mode one must be seriously considered as the solution. Indeed, previous studies successfully demonstrated the greatness of these accumulation devices over the conventional ones: higher speed [2], higher reliability and lower variation [3]. Furthermore, it has been verified that the noise level has been reduced by one order of magnitude in favor of the accumulation mode p-MOSFETs [4] and we propose here to finish the evaluation of this promising new technology with the evaluation of the noise performances of accumulation mode n-MOSFETs and the study of the noise sources.

2. Experiment and Results

The difference between an accumulation mode n-MOSFET such as the one depicted in Fig. 1b and an inversion mode n-MOSFET such as the one showed in Fig. 1a lies in the type of dopant impurity implanted inside the Poly-Silicon of the gate stack and the Silicon-On-Insulator (SOI). Therefore, contrary to the conventional inversion mode transistor, the current inside an accumulation mode one owes to the majority carriers.

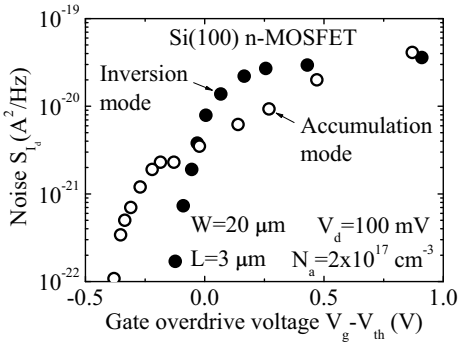

Fig. 2 1/f noise of an accumulation and inversion mode n-MOSFETs.

Actually, at low gate voltage, the SOI layer of an accumulation mode n-MOSFET is entirely depleted and the current is exclusively coming from the majority carriers confined at the back interface. While the gate voltage is increased, this layer vanishes and the SOI layer becomes neutral and therefore acts like a conductive material. A further increase of the gate voltage leads to the creation of an accumulation layer at the Si/SiO_2 front interface below the gate stack. As a result, the latter current adds to the SOI layer one to form the total current. n-MOSFETs working on accumulation and inversion mode have been fabricated on 50 nm thick (100) crystallographic oriented SOI. Their low frequency noise has been measured and the result is presented in Fig. 2. For negative gate overdrive voltages, the

best noise performances are found for the conventional inversion mode n-MOSFET. However, a transistor is generally used within the higher range of bias conditions and consequently the lower noise level encountered in favor of the accumulation mode MOSFET for positive gate overdrive voltages testifies of its merit for practical uses. This result combined with those already demonstrated during previous works [2-4] clearly confirm the superiority and the seriousness of a CMOS technology entirely based on accumulation mode MOSFETs as replacement of the present technology. The investigation has been moved forwards in order to analyze the noise sources. The modeling of the noise of the inversion mode n-MOSFET has been achieved within the oxide charge and induced mobility fluctuations, ascribing the origin of the noise to traps located inside the silicon oxide close to the Si/SiO_2 front interface [5]. In the case of the accumulation mode transistor, several regions are contributing to the total current and the evaluation of their respective noise requires a separate analysis. As showed in Fig. 3, the impact of the SOI layer on the measured capacitance is visible. It has therefore been used to evaluate the thickness of the depleted region of the SOI layer. So, the knowledge of the thickness of the conductive part of the SOI layer allowed the calculation of its current as a function of the gate voltage, which has been eventually subtracted from the measured current in order to extract the current generated at the back and front interface.

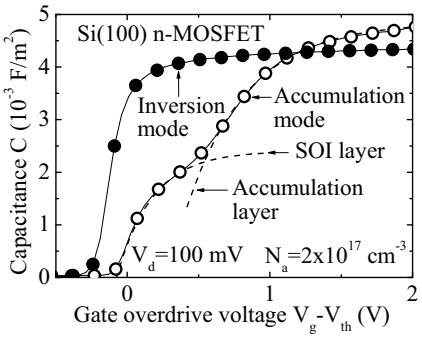

Fig. 3 Measured capacitance of accumulation and inversion mode n-MOSFETs.

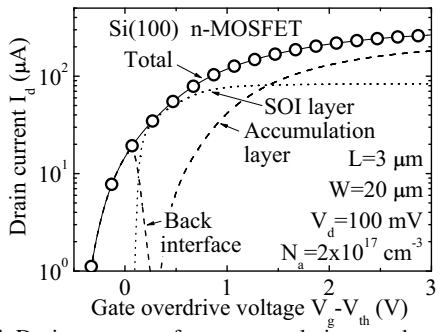

Fig. 4 Drain current of an accumulation mode n-MOSFET and its several contributions.

The modeling of each current has been reported in Fig. 4. Finally, the noise generated by each region, back interface, accumulation layer at the front interface, SOI layer and source and drain contacts has been calculated and the result is presented in Fig. 5. The noise stemming from the back interface and from the accumulation layer has been ascribed to the interface traps located respectively at the BOX/n-SOI and front n-SOI/SiO_2 interfaces while the one stemming from the SOI layer and the source and drain contacts has been attributed the fundamental fluctuations of the mobility of the Hooge theory [6]. At high bias their sum perfectly matches the experimental data. This result confirms the trend already revealed for the accumulation mode p-MOSFETs: compared to inversion mode MOSFETs, the noise reduction in favor of the accumulation ones will be even more efficient with a further increase of the doping concentration of the SOI layer since the accumulation layer will be generated at higher gate bias [2]. Additionally, contrary to the accumulation mode p-MOSFETs, the four previously described noise contributions could not explain the noise over the whole range of study.

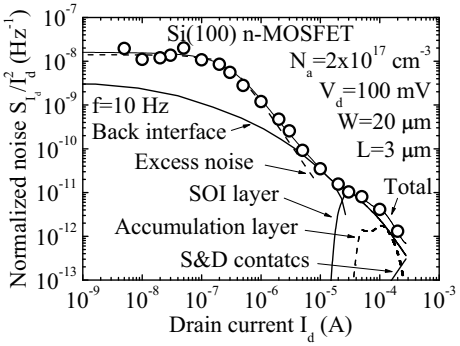

Fig. 5 Normalized noise of an accumulation mode n-MOSFET and its several contributions.

Indeed, the mismatch revealed the presence of an excess noise at low gate bias that has been confirmed trough the study of different gate sizes.

3. Conclusions

The present work shows that within the working range of a transistor, accumulation mode n-MOSFETs address more efficiently the noise issues than inversion ones. This efficiency might be even improved by suppressing the excess noise revealed at low drain current. Consequently, n- and p-accumulation mode MOSFET have all the assets to replace the present CMOS technology.

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