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SONNOS Nonvolatile Memory Based on Ultra-Thin Body Poly-Si Junctionless Field-Effect Transistor with Excellent Retention

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Abstract

This work presents the structure Junctionless FinFET(JL-FinFET) based on ultra-thin body (UTB) with double stacked Si_3N_4 charge trapping layer (NN-CTL) Si-SiO_2-Si_3N_4-Si_3N_4-SiO_2-Si (SONNOS) nonvolatile memory (NVM). The device shows excellent transistor performances including steep sub-threshold swing (SS) of 76 mV/dec, favorable V_{th}, and high I_{on}/I_{off} ratio (>10^7). For n-channel device, it shows excellent memory characteristics, high program/erase (P/E) performance, good endurance (>10^4 cycles) and an excellent 95~99% electron retention at 85℃ for 10 years.

1. Introduction

Recently, the concept of the junctionless field-effect transistor (JL-FinFET) device, which can avoid the using of complex source and drain doping engineering, has received considerable attention [1]-[3]. The proposed device structure provides the UTB [4] which reveal excellent performances of NVMs. However, erasing performance and data retention are still challenges in NVM research. Therefore, we firstly provide a simple double and high performance stacked Si_3N_4 (NN-CTL) SONNOS NVM based on JL-FinFET to explore the future application.

2. Device Fabrication

Fig.1(a) presents the gate stacked; one CTL is double stacked Si_3N_4 (NN=3nm/3nm). Fig.1(b) displays the process of fabrication for the JL-SONNOS NVMs. The device was fabricated by initially growing the 40-nm-thick poly-Si layer with adoption of solid-phase recrystallization (SPC) method. The n-channel and p-channel of poly-Si layer were implanted with phosphorous and BF_2 ions at dose of 1×10^{14} cm^{-2} by 16keV and 30keV, respectively. While serving as a channel, the active NWs channel was patterned by e-beam lithography and transferred by reactive-ion etching (RIE). Next, thermal oxidation was performed to produce the tunnel oxide with a 3 nm thickness. Additionally, 3 nm/3 nm of Si_3N_4 /Si_3N_4 trapping layer were deposited by LPCVD and the double stacked Si_3N_4 were designedly deposited separately with the 10 minutes interval during the time the step of broken vacuum in LPCVD is conducted. Subsequently, a 10 nm-thick TEOS oxide layer was deposited as a blocking oxide. Furthermore, 150 nm in-situ doped n^+ poly-Si deposition was performed as a gate electrode and patterned by e-beam lithography and RIE. Finally, the passivation and metallization were performed and sintered.

3. Results and Discussion

Fig.2(a) presents transmission electron microscopic (TEM) image of JL-FinFET SONNOS NVM with 2.2 nm thickness of UTB channel and 85 nm effective width of each NW. The TEM image in fig.2(b) shows the cross section of double stacked Si_3N_4 (3.5 nm/2.7 nm) structure with clear interface defects, and the diameter of each layer.

Fig.3 shows the I_D-V_G curve of n-channel and p-channel JL-FinFET with 0.2 μm L_G. As a result, the n-channel device possesses a better SS and lower DIBL than that p-channel device does. The excellent off-state characteristics of the gate is owing to full depletion of carriers in the UTB channel with 2.2 nm thickness.

Fig.4 plots the I_D-V_G characteristics of the JL-FinFET with SONNOS structure and different L_G from 0.2 μm to 0.5 μm. The JL-FinFET device shows a steep SS (76 mV/dec.) with 0.5 μm L_G, high I_{on}/I_{off} ratio >10^7 owing to better control of gate.

In NVM study, Fig.5 describes the Fowerler–Nordheim (FN) tunneling at (a) program and (b) erasing I_D-V_G curves of the n-channel JL-FinFET SONNOS NVM. The large ΔV_{TH} of devices are 4.9V and 5.3V after P/E presented.

Fig.6 shows a comparison of the SONNOS structure P/E characteristics of (a) n-channel and (b) p-channel JL-FinFET SONNOS NVM. The n-channel JL-FinFET SONNOS NVM possesses the larger memory window (ΔV_{TH}) than that p-channel does.

Fig.7 shows the endurance characteristics of n-channel JL-FinFET and n-channel JL planar of SONNOS NVMs. The ΔV_{TH} exhibits an upward trend and memory window closing of planar device. This result reveals that there are no sufficient number of holes which can compensate electrons in the trapping layer for every P/E cycle. In contrary, JL-FinFET SONNOS devices possesses large electrical field of NW corner and the sufficient numbers of holes can compensate electrons by electrical filed enhancing FN tunneling. The FinFET devices show better endurance than that of planar.

Fig.8 indicates that the retention characteristics for both of the JL-FinFET and JL-planar of SONNOS NVMs can maintain almost 95%~99% memory windows for 10 years, owing to numerous and deep interface traps of the middle of double stacked Si_3N_4 (NN) layers. The interface traps artificially generated by the disorder double stacked Si_3N_4 layer might play the deep traps which prevent electrons from outflowing.

4. Conclusion

This work demonstrates both high performance in transistors and memory characteristics of the JL-FinFET SONNOS NVM. The numerous and deep interface traps artificially generated by the double stacked Si_3N_4 (NN) layers improve the erasing and retention properties. In short, JL-FinFET SONNOS NVM is suitable for application of future 3D NAND flash memory.

Acknowledgements

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References

[1] P. Singh, et al. , IEEE Electron Dev. Lett. **32** (2011) 1752.
[2] J.-P. Colinge, et al., Appl. Phys. Lett. **94** (2009) 053511.
[3] R. Rios, et al. IEEE Electron Dev. Lett. **32** (2011) 1170.
[4] S.-Y. Kim et al., VLSI Tech. Dig. (2014) 115.

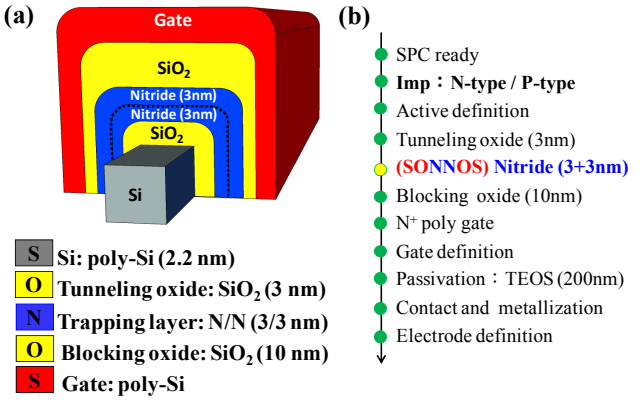

Fig. 1 The device structure for JL-FinFET SONNOS NVM. (a) The cross section of charge-trapping layer. (b) The process flows of the fabrication in the SONNOS NVM

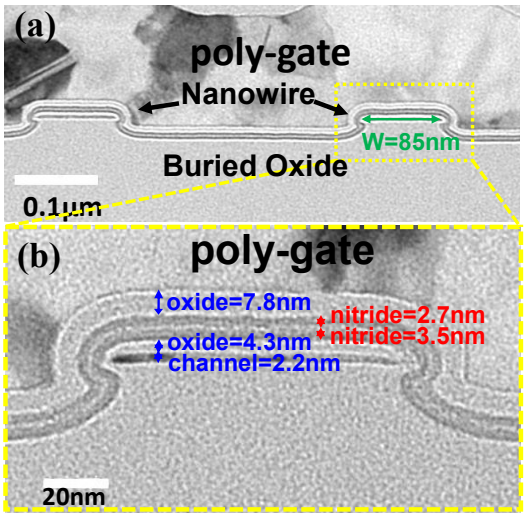

Fig. 2 (a) TEM image of NWs. (b) Magnified TEM image of the SONNOS with Poly-Si channel(2.2nm) SiO_2(4.3nm)/Si_3N_4 (2.7nm/3.5nm)/SiO_2(7.8nm).

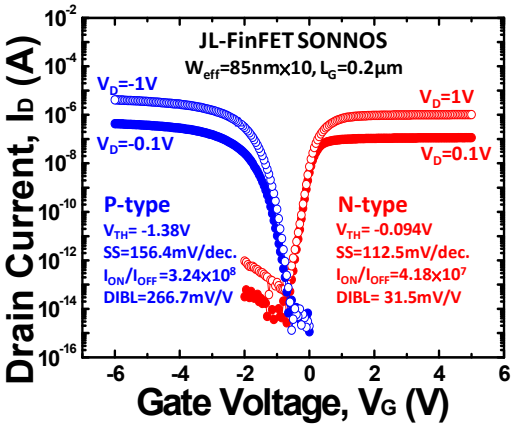

Fig. 3 I_D-V_G curves of n-ch. and p-ch. JL-FinFET SONNOS.

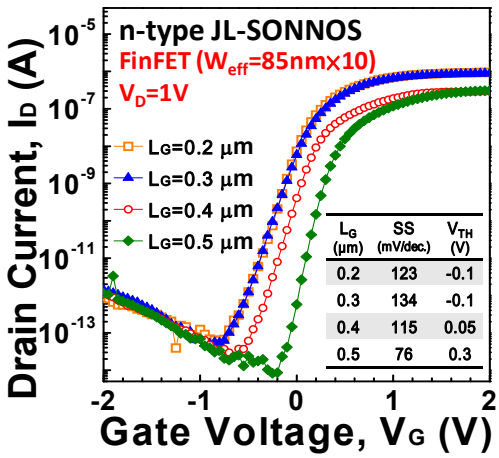

Fig. 4 I_D-V_G curves of JL-FinFET SONNOS NVMs for L_G=0.2μm to L_G=0.5μm.

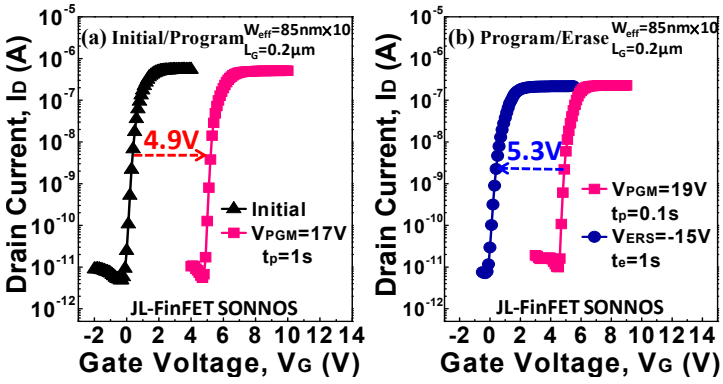

Fig. 5 (a) FN programming, and (b) FN erasing hysteresis curves of the n-channel JL-FinFET SONNOS NVM.

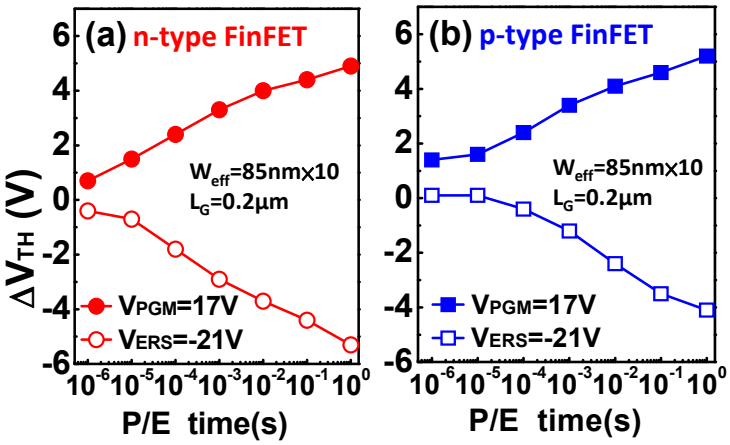

Fig. 6 P/E performance of (a) **n-channel** JL-FinFET (b) **p-channel** JL-FinFET SONNOS NVM.

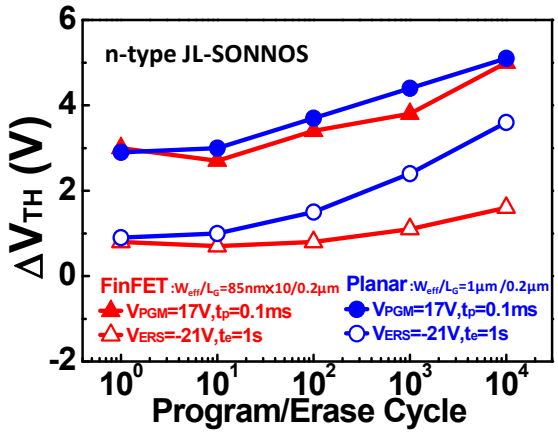

Fig. 7 Endurance performance of n-ch. JL-FinFET and n-ch. JL planar SONNOS NVMs.

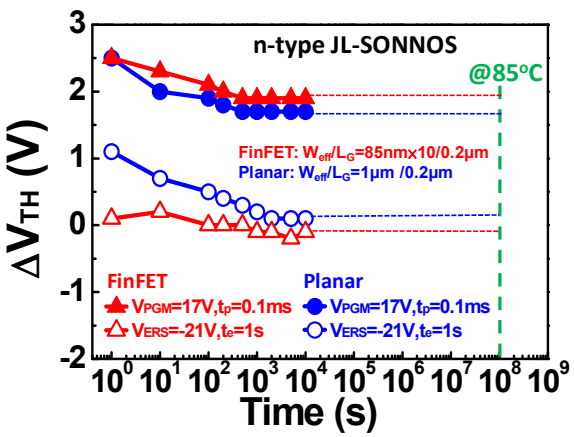

Fig. 8 Retention of JL-FinFET and JL planar SONNOS NVMs.