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Resistance switching memory operation of $CaF_2/Si/CaF_2$ resonant-tunneling quantum-well structures using nanocrystalline-Si secondary barrier layers

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Abstract

A novel resistance switching memory using $CaF_2/Si/CaF_2$ resonant-tunneling quantum-well (QW) heterostructures sandwiched by nanocrystalline Si (nc-Si) as secondary barrier layers has been proposed and the room-temperature resistance switching memory pulsed operation has been demonstrated for the first time without using CdF_2 as a component material. Material parameters such as effective mass and conduction band discontinuity (ΔE_C) for atomically thin CaF_2 layers are also discussed.

1. Introduction

The dimensions of the elements comprising integrated circuits have been decreasing to the nanoscale. One essential building block for nanoscale solid-state devices is electric potential sequences for realizing electronic functions such as electron injection, transport, and storage, which can be implemented using the energy band discontinuity at atomically abrupt heterointerfaces. A CaF_2/Si heterostructure is an attractive candidate for application to Si-based integrated devices, such as resonant-tunneling diodes (RTDs)[1,2] and transistor, coulomb blockade devices, because of the large conduction band discontinuity (ΔE_C~2.3 eV)[3,4] at the heterointerface and the small lattice mismatch with silicon owing to the similar cubic-based crystalline structures. Owing to the large ΔE_C and energy band gap (E_g for CaF_2 is 12.1 eV[5,6]), the leakage current is expected to be suppressed to a low level even at room temperature (RT) and, moreover, the voltage for tunneling transport can be controlled by utilizing a multiple-quantum-well tunneling scheme, such as resonant tunneling or sequential tunneling, with appropriately designed quantum-well (QW) layer thickness sequences. In this study, we have proposed novel configuration of resistance switching memory using $CaF_2/Si/CaF_2$ quantum-well structure sandwiched by nanocrystalline Si (nc-Si) secondary barrier layers and demonstrated pulsed resistance switching memory cyclic operations at RT.

2. Experiment

Figure 1 shows the schematic device structure and band diagram (flat band) used in this study. The device comprises a $CaF_2/Si/CaF_2$ double-barrier resonant-tunneling (DBRTD) structure and nc-Si layers as secondary energy barriers, that sandwich the DBRTD structure. The CaF_2 layers mainly act as resonant-tunneling barriers for charge injection and ejection between a Si-QW and a reservoir of electrons. The nc-Si layers with a wider band gap than that of Si act as energy barriers to prevent electrons from escaping from the confined state in the Si-QW. The upper n-type As-doped nc-Si layer also acts as an emitter of electrons to be injected.

An 80-nm-thick SiO_2 layer was formed by wet oxidation on a p-type Si(111) substrate with a 0.1° off miscut angle and a resistivity of less than 4 mΩ·cm. Subsequently, 2-μm-diameter holes were formed by photolithography and wet chemical etching. Subsequently, a protective oxide layer was formed on the Si surface at the bottom of the hole by boiling in a solution of SC2. After loading into an ultra-high-vacuum (UHV) chamber, nc-$Si/CaF_2/Si/CaF_2$/nc-Si multilayered structures were grown on the bottom Si by a molecular beam epitaxy (MBE)-based technique[7,8]. The first 2.2-nm-thick nc-Si layer was grown by codeposition using a Si molecular beam via electron-beam evaporation together with a partially ionized CaF_2 beam to obtain an atomically flat nc-Si layer at a substrate temperature (T_s) of 80 °C. The flux ratio of $Si:CaF_2$ is fixed to 1:1 in this study; this ratio strongly affects the band gap and conductance of nc-Si layers. Subsequently, a 0.9-nm-thick CaF_2 layer was grown, followed by Si-QW growth at T_s = 80 °C[9,10]. In this study, three samples with Si-QW layers of different thicknesses (W = 2.5, 2.8, 3.1 nm) were prepared. The thickness of the Si-QW layer significantly affects the voltage for the peak current (V_{peak}), which corresponds to the quasi-energy levels in the Si-QW. Finally, the top nc-Si layer was grown with As flux as an n-type dopant. This resulted in an As atomic density of 10^{19} cm^{-3}. After the growth, *in situ* annealing was carried out at 650 °C for 30 min to improve the crystalline quality. After unloading each sample from the UHV chamber, 200 × 200 μm^2 square Au/Al electrode pads were formed by lift-off.

3. Results and discussion

Figure 2 shows I-V curves exhibiting the bipolar resistance switching cycle at RT of the samples with the Si-QW layer of W = 2.8 nm. The switching voltage V_{peak} (the voltage for the state transition from the LRS to the HRS) was approximately 1.0 V and the peak current density J_{peak} was 48 kA/cm^2. The ON/OFF current ratio was approximately 2.8. Note also that the V_{peak} value of nearly 1 V was in the range of values derived by simple theoretical analysis of the I-V curve of an RTD using a ballistic transport model and by the transfer matrix method for the

tunneling probability based on the effective mass approximation and the Esaki-Tsu formula for the calculation of the I-V curves[11] under the assumption that ΔE_C(nc-Si/Si) is around 0.29 eV, which is about half the value derived from the discussion based on the optical absorption measurement.

Figure 3(a) shows plots of the mean value of V_{peak} indicated by solid diamonds with error bars as a function of the Si-QW thickness, where one monolayer (1 ML) of Si corresponds to 0.31 nm and therefore, W = 8 ML corresponds to a thickness of around 2.5 nm, 9 ML to 2.8 nm, and 10 ML to 3.1 nm. Although the distribution of V_{peak} is broad, the mean values of V_{peak} were well reproduced by the simple theoretical model, as plotted by the solid triangles, strongly indicating the semi-quantitative validity of device modeling when using modified material parameters for atomically thin CaF_2[12] Current responses for input voltage pulse sequences of periodic write-read-erase-read memory cycle operation were clearly demonstrated at RT for the sample with the Si-QW layer of W = 2.8 nm (9 ML). Figure 3(b) shows plots of current for high resistance state (I_{HRS}) and for low resistance state (I_{LRS}) as a function of the number of memory cycles. Over 28000 memory cycles with perfect separation of I_{HRS} and I_{LRS} and no error were observed. These results clearly confirmed that the memory cycle operation of the proposed device is multiply reversible and reproducible, at least in principle, although further improvement is required to enable practical applications of memory systems.

3. Conclusions

In conclusion, we have proposed and demonstrated a novel resistance switching memory consisting of nc-Si/CaF_2/Si/CaF_2/nc-Si resonant-tunneling QW structures grown on Si(111) substrates without the need to use CdF_2 as a component material. A clear resistance switching memory cycle was observed at RT for the samples with Si-QW layers of 2.5, 2.8, and 3.1 nm thickness. A typical switching voltage of lower than 1 V, a peak current density of 26–930 kA/cm^2, and an ON/OFF ratio of approximately 1.2–41 were obtained. A stable current response for the repeated input pulse of the memory cycle operation was observed for 28000 cycles. The device operation concept and configuration philosophy based on the band engineering of artificial nano-heterostructures proposed in this study are a possible candidate for new nonvolatile memories or a ReRAM scheme for future LSI technologies aimed at ultimate scaling down to the nanometer scale.

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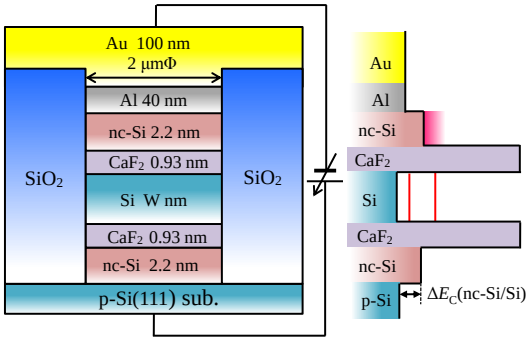

Fig. 1 Schematic cross section of the device structure and band diagram in flat band condition.

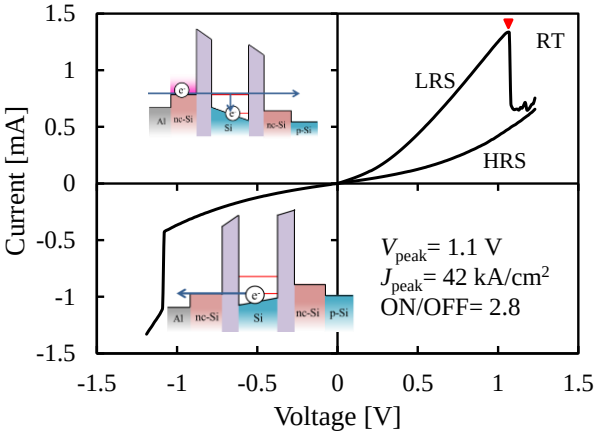

Fig. 2 Room temperature I-V curve of a resistance switching memory cycle.

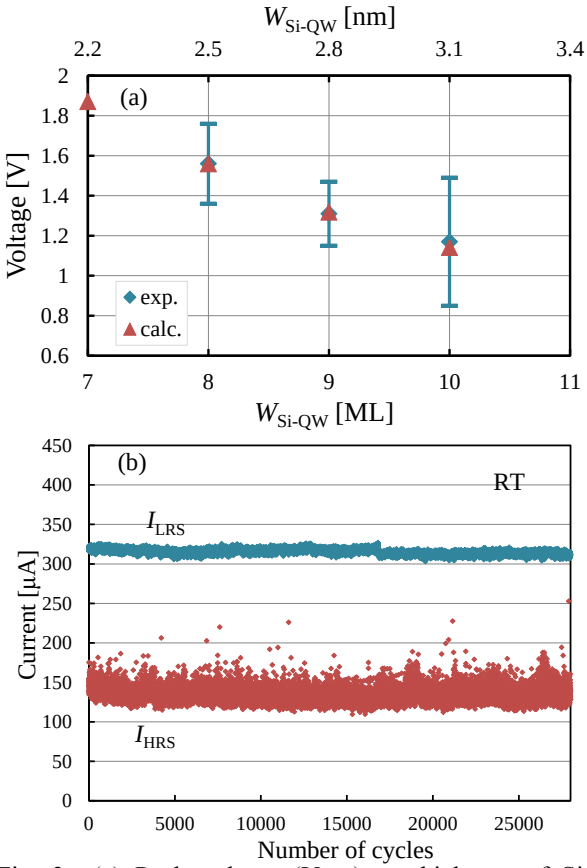

Fig. 3 (a) Peak voltage (V_{peak}) vs thickness of Si-QW (W_{Si-QW}). (b) Current response for pulsed memory cycles.