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Guideline Model for the Bias-Scheme-Dependent Power Consumption of a ReRAM Crossbar Array

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Abstract

The power consumption of a resistive random access memory (ReRAM) crossbar array can vary according to the nonlinearity of a selector device. In this paper, the power consumption for different bias schemes and characteristics of a selector device is investigated. Power consumption is analyzed by dividing the area of the array, and a guideline model for the required nonlinearity characteristics of a selector device, which guarantees lower power consumption for a 1/3 bias scheme compared with a 1/2 bias scheme, is proposed. The results of the analytical model correspond well with the crossbar array simulation results. Therefore, the nonlinearity requirements of a selector device for low power consumption for a 1/3 bias scheme can be immediately obtained using this guideline model without crossbar array simulation.

1. Introduction

The crossbar array architecture is one of the most promising structures among various 3D stacking technologies for constructing high-density memories [1]-[2]. Resistive random access memory (ReRAM) has simple two-terminal structures that are compatible with crossbar arrays [3]-[4]. In these arrays, a strong nonlinearity using a selector device is required to prevent leakage current or sneak path current [5]. However, theoretical investigations are insufficient for exploring the relationship between a selector device and power consumption in ReRAM crossbar arrays. The aim of this study is to demonstrate that the power consumption of a crossbar array can be changed by the nonlinearity of a selector device and to propose a new power consumption model that is derived from the nonlinearity characteristics of the selector device.

2. Device Model

In this study, the crossbar array architecture consists of a selector device and a resistor (1S+1R cell architecture) for ReRAM. The turn-on voltage of the resistor V_{set}, is 1.0 V, and the turn-on voltage of the selector V_{th}, is 1.5 V. The selected word line is forced to V_{dd}, and the selected bit line is biased to the ground for all bias schemes. The unselected word lines is set to $V_{dd}/2$ for the 1/2 bias scheme and to $V_{dd}/3$ for the 1/3 bias scheme. Similar to the unselected word line, the unselected bit line is biased to $V_{dd}/2$ and $2 \times V_{dd}/3$, for the 1/2 bias scheme and the 1/3 bias scheme, respectively. To investigate the power consumption, various HSPICE simulations were performed for different nonlinearity characteristics of the selector device. The inset of Fig1 shows the off characteristics of the selector device, which is modeled by the hyperbolic sine function as [6]

$$I_{selector} = \gamma \cdot \sinh(\alpha \cdot V), \qquad (1)$$

where γ and α represent a conductance parameter and the nonlinearity of the selector device, respectively. The nonlinearity characteristics of a selector are defined as the subthreshold slope (SS), which is the reciprocal of the IV curve slope as $SS=\Delta V_{selector}/\Delta(\log I_{selector})$. Fig. 1 shows the total power consumption according to the array size, SS, and bias schemes. The array used in our simulation is an $n \times n$ square matrix, where n is the number of word lines or bit line. To consider the worst case, we select the "worst corner cell" that is located furthest from the voltage sources; all cells exist in a low-resistance state or on state.

As shown in Fig. 1, the power consumption increases with the array size and SS of the selector device for all bias schemes. The power consumption of a 1/3 bias scheme is larger than that of a 1/2 bias scheme because all unselected cells are biased to $V_{dd}/3$ in the 1/3 bias scheme. However, the power consumptions of a 1/3 bias scheme and 1/2 bias scheme are similar in small array size. Therefore, the SS of a selector must be small to minimize the power consumption of a 1/3 bias scheme.

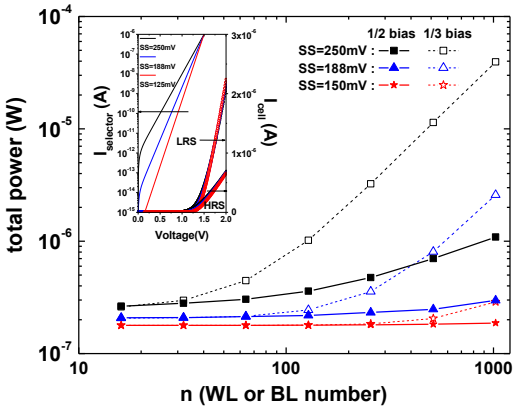

Fig. 1 Total power consumption according to the array size, SS of the selector, and bias schemes at V_{dd}=1.5V. (Inset graph: I-V characteristics of 1S and 1S+1R)

3. Power Model

To clarify the difference in power consumption with a bias scheme, power consumption is compared by dividing the area of the array. Fig. 2 shows a schematic representation of an $n \times n$ crossbar array. In the case of a 1/3 bias scheme, the area is classified to two regions: the selected cell and unselected cells. The half-selected cells must be separated from the unselected cells in a 1/2 bias scheme due to the potential difference between half-selected cells and unselected cells. As shown in Fig. 3, the total power consumption is primarily induced from unselected cells for a large array size in the 1/3 bias scheme. Conversely, the total power consumption is caused by half-selected cells in the 1/2 bias scheme. Therefore, the relationship between the total power dissipation and array size for each bias scheme can be simplified as

$$P_{1/3} \approx (n^2-1)\cdot\frac{V_{dd}}{3}\cdot I_{1/3}, \qquad (2)$$

$$P_{1/2} \approx 2(n-1)\cdot\frac{V_{dd}}{2}\cdot I_{1/2}, \qquad (3)$$

where $P_{1/3}$ and $P_{1/2}$ are the total power consumptions for the 1/3 bias scheme and the 1/2 bias scheme, respectively. $I_{1/3}$ and $I_{1/2}$ are the currents of the unselected cells and half-selected cells, respectively. Equation (2) and (3) are compared and modified to

$$\frac{P_{1/3}}{P_{1/2}} = \frac{(n+1)}{3}\frac{I_{1/3}}{I_{1/2}} \leq 1. \qquad (4)$$

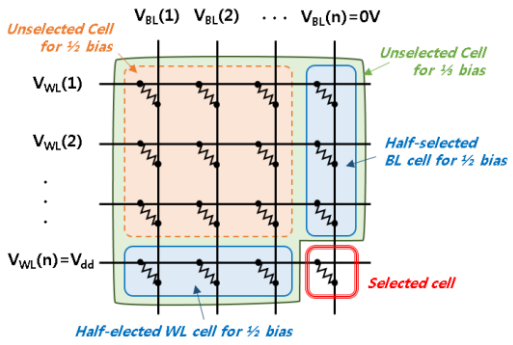

Fig. 2 Illustration of an $n \times n$ crossbar array.

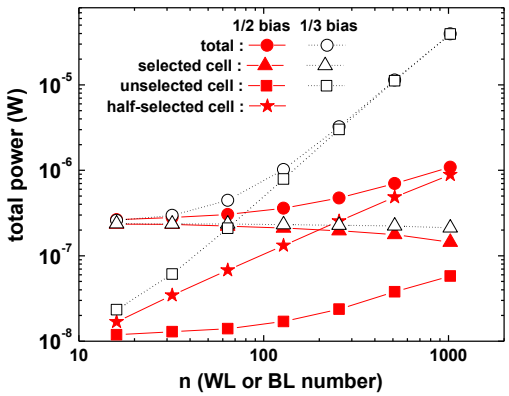

Fig. 3 Power consumption with (a) 1/2 and (b) 1/3 bias schemes at each region; selected cell, half selected cells, unselected cells. Selector SS =250mV, V_{dd}=1.5V.

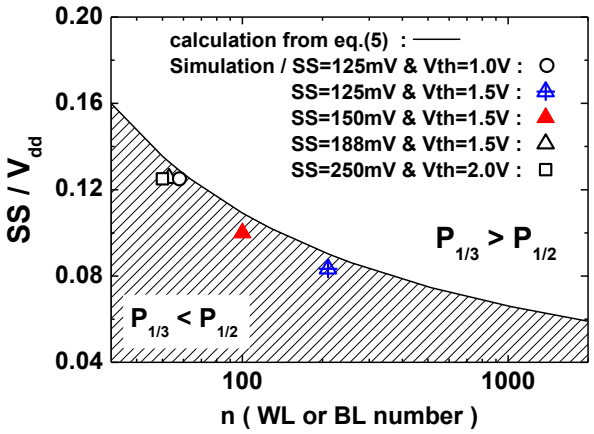

Fig. 4 SS/V_{dd} with various SS and V_{th} of selector. The line represents the calculation result from Equation (5).

Using (4) and the definition of the SS, the new conceptual model for power consumption can be derived as

$$\frac{SS}{V_{dd}} \leq \frac{1}{6\cdot log\left((n+1)/3\right)}. \qquad (5)$$

Therefore, (5) is the guideline model for the nonlinearity characteristics of selector device to guarantee that a 1/3 bias scheme consumes less power than 1/2 bias scheme.

As shown in Fig. 4, we compared the calculation result of (5) with the simulation results to confirm the validity of (5). In Fig. 4, the solid line represents the solution of (5) in the equality condition and the symbol represents the results of the crossbar array simulation. The crossbar array simulation results show good agreement with (5). In addition, our guide-line model is consistent with the crossbar array simulation results for various selectors with different V_{th}. Therefore, our model will be helpful for obtaining the nonlinearity characteristics of a selector device for low-power consumption in a 1/3 bias scheme.

4. Conclusions

This study analyzes the power consumption of a crossbar array for various selector device characteristics and bias schemes. The new guideline model for power consumption, which is derived from the nonlinearity curve of the selector device, is proposed. This model exhibits excellent accuracy compared with the HSPICE simulation results. Therefore, the suggested power guideline model for crossbar array can be used to determine the nonlinearity characteristics of a selector device and estimate the power characteristic in large array size, without crossbar array simulation.

References

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