Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp148-149

# Non-volatile and Volatile Hybrid Memories Embedded in the Standard CMOS Process

Yi-Lin Chiou, Hongchin Lin, Hou-Jen Chiu and Chia-You Wu

Dept. of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan
Phone: +886-4-2284-0688 ext. 250 E-mail: hclin@ nchu.edu.tw

**Abstract**

**A differential PMOS multiple-time programmable and SRAM hybrid memory is proposed using the 0.18μm CMOS logic process without additional process steps. Hot carriers based program and erase mechanisms make low voltage operation possible and were confirmed by measurement.**

## 1. Introduction

In recent years, many emerging non-volatile memories (NVM) combined with volatile memories and their circuit applications were proposed. For example, the SONOS based flash memories are integrated with SRAM cells [1], magnetic tunnel junctions (MTJ) are embedded with SRAM [2] or DRAM [3], and resistive memory (memristor) based nonvolatile SRAM cells have been proposed [4, 5]. Their advantages are fast read/write, numerous cycle times, low power, and possibility to be integrated with CMOS processes. However, the non-volatile components need unique and extra process procedures, and thus fabrication cost is increased, as well as yield may be degraded.

To avoid additional process costs, the differential multiple-time programmable (MTP) NVM has been proposed using the standard CMOS logic process without extra process steps [6, 7]. However, both of them employ Fowler–Nordheim tunneling (FNT) to erase or/and program data. FNT usually requires more than 10V for operation, which increases peripheral circuit complexity in the standard CMOS processes. Here, the new operation of the MTP NVM integrated with SRAM is proposed using 7nm gate-oxide 3.3V I/O devices biased at much less than 10V for program and erase in the 0.18μm CMOS logic process.

## 2. Hybrid Memory Circuit

Figures 1 (a) and (b) show the top view and the schematic of the MTP with SRAM hybrid memory circuit, respectively. The bold lines in Fig. 1 (a) represent connection between transistors using metal wires. The differential MTP memory is composed of 3 PMOS transistors on the same N-well (NW) with two PMOS based coupling gates tied to their N-wells denoted as CG. FG0 and FG1 are acted as the floating gates to store charges. The SRAM comprises the five NMOS transistors plus the 3 PMOS transistors used in the MTP operation.

To program the differential MTP memory, CG and SG are set to 0, and one of floating gates is selected. For instance, if FG0 is the one to be programmed, 3V and -3V are applied on the source line (SL) and BL0/b0, respectively. Since g0 is 0V to allow -3V passing to Qb, the holes flow from SL to Qb and hot carriers near Qb are produced owing to impact ionization. Then, the channel hot holes are injected into FG0 to raise the magnitude of threshold voltage ($|V_{th\_high}|$). In the mean time, BL1 and b1 are biased at 0V, which makes FG1 unchanged. To erase the charges in FG0, the bias conditions remain the same except CG biased to 6V. Owing to high reversed bias between the drain and the body of the FG0 PMOS transistor, punch-through assisted hot electrons are generated near the drain. Those hot electrons may be injected into FG0 to lower the magnitude of threshold voltage ($|V_{th\_low}|$). Table I lists the bias conditions of program, erase and read for MTP operation, as well as write and read for SRAM operation.

The read procedures for both of the MTP and SRAM are almost identical. Firstly, g0 and g1 turns off the 2 corresponding NMOS transistors, while BL0 and BL1 are equalized at low voltages like 0V. The data at Q and Qb are developed for the MTP. Those data are already there for the SRAM. After g0 and g1 switch on the NMOS transistors, the correct data appears at BL0 and BL1. To evaluate the data holding ability of SRAM, static noise margin (SNM) simulation result is shown in Fig. 2. The maximum square to fill in the butterfly curve is about 1V.

## 3. Experimental Results

The drain current of the 2 PMOS transistors FG0 and FG1 were measured by turning off the SW NMOS transistor. Figure 3 (a) compares the read currents from BL0 and BL1 through Transistors FG0 and FG1 before and after FG0 is programmed. After hot holes are injected into FG0, the current difference between BL0 and BL1 reaches 8μA at SG = 1.8V. Figure 3 (b) shows the current difference between BL0 and BL1(Before) becomes less than 2μA after erase. Then, after FG1 is programmed, the current difference increases to 6μA.

The current difference of repeated program and erase (P/E) cycles is shown in Fig. 4 at SG=1.8V. The average current different at the programmed state is about 7μA, while very small current difference is observed after erase.

To demonstrate the read operation, Fig. 5 is the waveforms for the programmed MTP read and equalized at BL0 and BL1 consecutively. Since g0 and g1 are biased at 3V, the voltage at BL0 can only reach 2.5V.

## 4. Conclusions

A differential MTP and SRAM hybrid memory was designed and measured using the 3.3V I/O devices in the 0.18μm CMOS process. We believe it is a cost-effective hybrid memory for low memory capacity applications.

**Acknowledgements**

The authors would like to acknowledge the Chip Implementation Center (CIC) of the National Applied Research Laboratories (NARL) of Taiwan for the support in chip fabrication. This work was supported by Ministry of Science and Technology of Taiwan (MOST 103-2220-E-005-005).

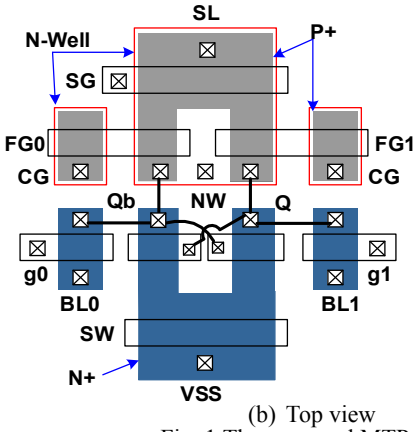
**References**

[1] M. Fliesler, D. Still, and J. M. Hwang, *Non-Volatile Semiconductor Memory Workshop, and International Conference on Memory Technology and Design. (Joint)* (2008) 83.
[2] T. Ohsawa *et al.*, *Symp. VLSI Circuits* (2012) 46.
[3] K. Abe *et al.*, *IEEE International Electron Devices Meeting (IEDM)* (2012) 10.5.1.
[4] S. Yamamoto, Y. Shuto, and S. Sugahara, *IEEE Custom Integrated Circuits Conference* (2009) 531.
[5] P. F. Chiu *et al.*, IEEE Journal of Solid-State Circuits **47** (2012) 1483.
[6] B. Wang *et al.*, IEEE Trans. Electron Devices **54** (2007) 2526.
[7] T.-L. Lee *et al.*, IEEE Electron Device Letters **32** (2011) 587.

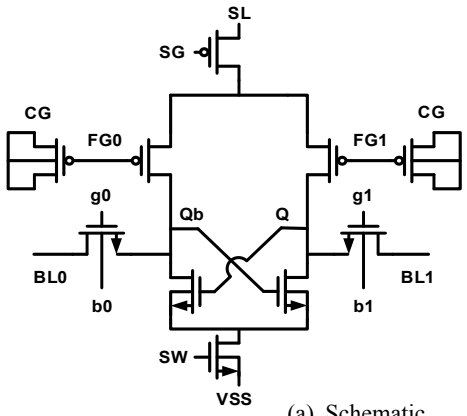
Table I Bias conditions of the hybrid memory

| | | SL | SG | CG | BL0 | BL1 | g0 | g1 | b0 | b1 | SW | VSS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MTP | Prog_1 | 3 | 0 | 0 | -3 | 0 | 0 | 3 | -3 | 0 | 0 | -3 |
| | Erase_1 | 3 | 0 | 6 | -3 | 0 | 0 | 3 | -3 | 0 | 0 | -3 |
| | Prog_0 | 3 | 0 | 0 | 0 | -3 | 3 | 0 | 0 | -3 | 0 | -3 |
| | Erase_0 | 3 | 0 | 6 | 0 | -3 | 3 | 0 | 0 | -3 | 0 | -3 |
| | Read | 3 | 0 | <1.8 | $\overline{out}$ | out | 3 | 3 | 0 | 0 | 3 | 0 |
| SRAM | Write | 3 | 0 | 0 | $\overline{in}$ | in | 3 | 3 | 0 | 0 | 3 | 0 |
| | Read | 3 | 0 | 0 | $\overline{out}$ | out | 3 | 3 | 0 | 0 | 3 | 0 |

(Unit: V)(NW = 3V)




(b) Top view




(a) Schematic

Fig. 1 The proposed MTP and SRAM hybrid memory.

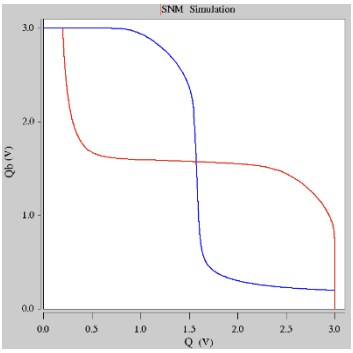
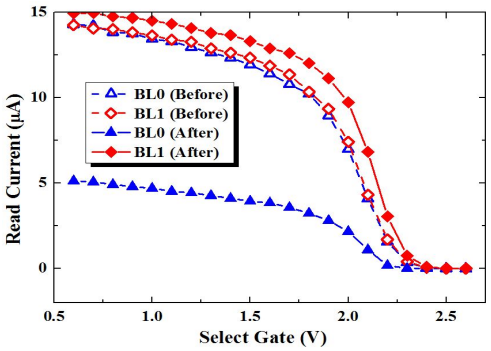
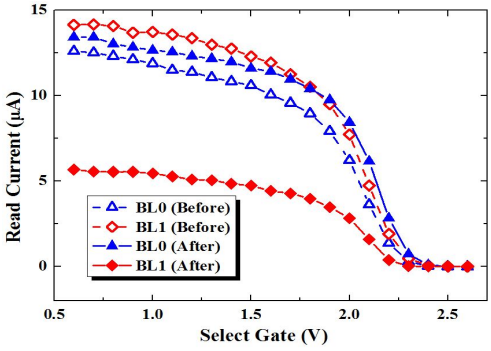



Fig. 2 The simulated SNM shows the butterfly cureve with the maximum square of 1V.




(a) Before (initial) and after FG0 is programmed.




(b) Before (FG0 erased) and after FG1 is programmed.

Fig. 3 Currents through FG0 and FG1 transistors

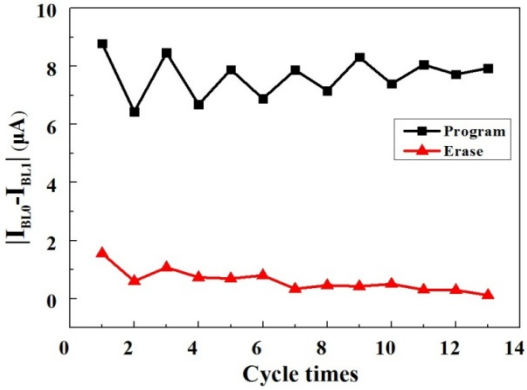



Fig. 4 The current difference of P/E cycles at SG=1.8V.

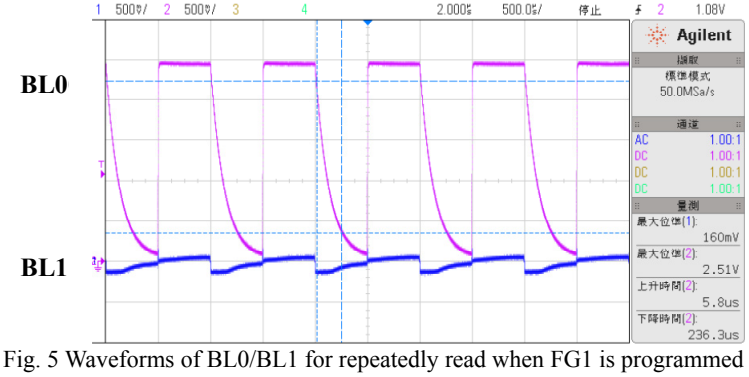



Fig. 5 Waveforms of BL0/BL1 for repeatedly read when FG1 is programmed