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A DC-balanced Bus-invert Coding for Stabilizing the Intermediate Power Level in Stacked-Vdd LSIs

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Abstract

A new parallel bus coding method to obtain the DC-balanced code with only one additional bit is proposed. The stabilization effect on the intermediate power level in the stacked-Vdd structure was experimentally confirmed by the measurement with two test chips.

1. Introduction

In recent LSIs with the down-scaled CMOS device, the supply voltage should be lowered to less than 1-V to satisfy the device reliability. Therefore the optimal supply voltages for LSIs are locally generated by the step-down regulator. As a result, it causes the wasteful power consumption and its heat production has an adverse effect to the neighboring LSIs. To overcome this problem, the stacked-Vdd circuit configuration by connecting the two (or more) circuit blocks in series between the power source and ground has been studied [1] [2]. However, with this structure, if there is a difference of the current consumption between the upper and lower circuit blocks, the voltage fluctuation of the Intermediate Power Level (IPL) is increased and a supporting regulator would be required to suppress the voltage fluctuation. We previously reported to eliminate the supporting regulator by stabilizing the voltage fluctuation of the IPL by using the 8B10B coding with toggle conversion circuits [3]. Although this method can always control the number of switching in the parallel bus to 5-bits, it requires two additional redundant bits for every 8-bit input signals.

In this paper, we propose a new coding method which achieves the same effect as the previous work with only one redundant bit to the wider parallel bus.

2. 8B10B Coding and Bus-invert Coding [4] [5]

The 8B10B coding method employed in Ref. 3 is widely used in the serial communication system, such as an optical fiber channel, high-speed Ethernet and USB [4]. It generates a 10-bit output code in which almost a 50% existence probability of '1's from an original 8-bit input code. Its binary running disparity control feature achieves to generate the 'DC-balanced codes', in which the number of '1's in the sequence of the output codes is strictly controlled to 5-bits.

On the other hand, the Bus-invert coding was proposed to halve the number of switching in a parallel bus by adding one redundant bit [5]. It contributes a 50% reduction of the simultaneous switching noise of CMOS I/Os, however it has no DC-balance capability.

3. DC-balanced Bus-invert Coding

In order to obtain the DC-balanced code with just one redundant bit, we tried to modify the Bus-invert coding system. In our previous work, the running disparity was binary value because of the 8B10B coding feature. On the other hand, in Bus-invert coding, the running disparity may vary from 0 to N. Therefore, we developed the multi-value running disparity (MVRD) control and adopted it to the Bus-invert coding system. Figure 2 shows the block diagram of the new encoding circuit to generate the DC-balanced code. The flowchart is also shown in Fig.3. In these figures, the circuit blocks and parts of the flowchart enclosed by the dashed boxes are the additional developed elements to accommodate the MVRD control feature to the conventional Bus-invert coding.

The procedure of new coding is as follows. First, the MSB of ‘0’ is added as a sign bit to the original N-bit code to generate a new N+1-bit code. Next, the bitwise differences between the new N+1-bit code and the output code in previous clock are examined by XOR gates, and then number of switching bits (NS) is counted. The majority voter circuit decides the SIGN bit which indicates whether the NS is more than N/2 or not, as the conventional bus-invert coding. Second, if the current MVRD value is less than N/2, SIGN bit is inverted. Finally, the output code is flipped depending on the polarity of SIGN bit, and the MVRD value is also updated depending on the SIGN bit and NS, as shown in Fig.3. This procedure guarantees that the obtained codes are DC-balanced codes in a finite interval. Fig.4 shows the coding examples for 8-bit input codes. In the input data, the average of NS (NS_ave) varies from 0 to 8. In the previous work, the NS_ave is controlled to 5.0 for any 8-bit input data. On the other hand, in our proposed coding, the NS_ave is controlled to be 4.0. This also means the 20% of I/O switching power reduction is achieved compared to the previous method.

Figure 5 shows the encoding / decoding circuits for the 32-bit parallel bus interface. The previous work requires the bundle of 8B10B coding circuits every 8-bit signals. On the other hand in new coding, it requires single encoder and decoder circuits and the additional I/O is just one bit. And the decoder circuit for new coding is quite simpler than the 10B8B decoder, because it is identical to the conventional Bus-invert decoder which consists of just XOR gates. The designed total transistor counts and the total I/O pins for the coding system for N-bit parallel bus system are summarized

in Fig.6. In the proposed coding, just one additional bit is always sufficient even for the wider bus. And the size of the circuit is much less than half of the previous work.

4. Measurement Results in Stacked-Vdd Structures

To verify the effectiveness of the proposed method by the measurement, we have developed a test chip with 0.18-um CMOS process as shown in Fig.7. Figures 8 (a)-(d) show the measured results of the fluctuation of the IPL in the stacked-Vdd structure using two test chips. In Fig.8 (a) and (b), the IPLs have DC bias shifts in the worst cases are observed in the case of without coding and with Bus-invert coding, respectively. Figure 8 (d) shows the result of proposed coding, the IPL has the slight fluctuations, however, it is successfully stayed in the middle of Vdd/Gnd (1.8-V) without DC bias, as well as the result of the previous work shown in Fig.8 (c).

5. Conclusion

We have proposed a new DC-balanced Bus-invert coding in which the multi-value running disparity (MVRD) control feature is integrated with just one redundant bit. Its DC-balanced feature and the stability of the IPL in the stacked-Vdd structure was experimentally confirmed by the measurements with two test chips

Acknowledgments

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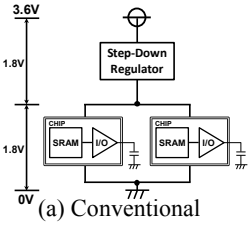
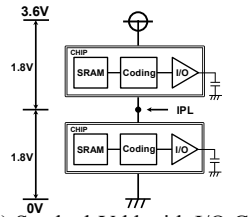


(a) Conventional



(b) Stacked-Vdd with I/O Coding

Fig.1 Circuit Configuration

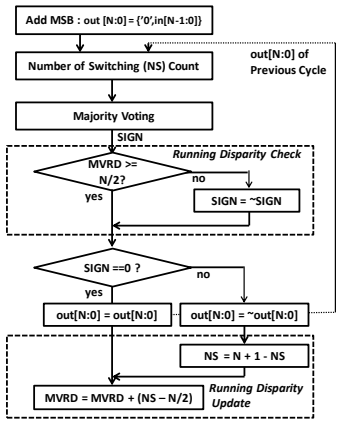


Fig.3 Flowchart of Proposed Coding

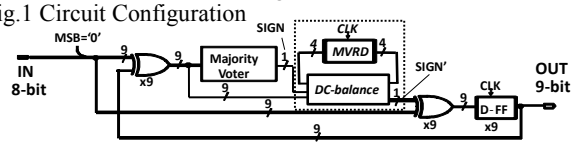
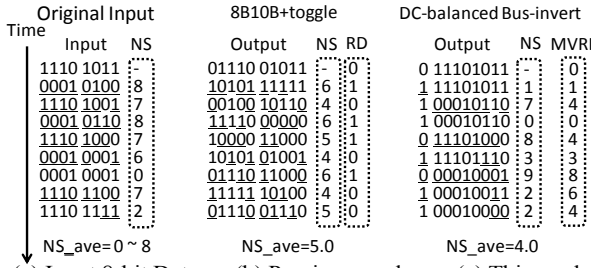
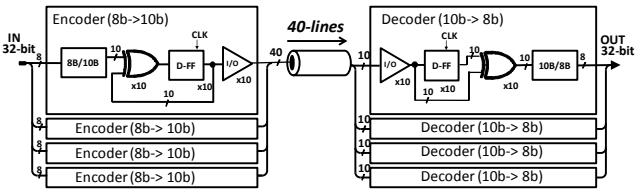


Fig.2 Block Diagram of Proposed Encoding Circuit for 8-bit bus

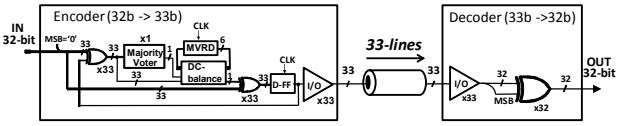


(a) Input 8-bit Data (b) Previous work (c) This work

Fig.4 Coding Examples



(a) 8B10B + toggle Conversion [3]



(b) This work : DC-balanced Bus-invert Coding

Fig.5 Coding System for 32b Bus

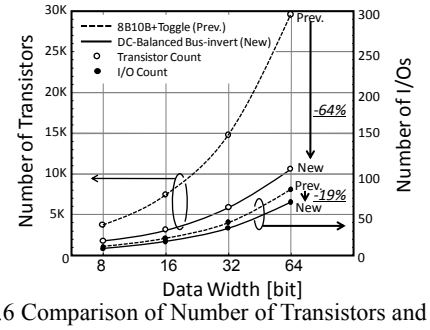


Fig.6 Comparison of Number of Transistors and I/Os

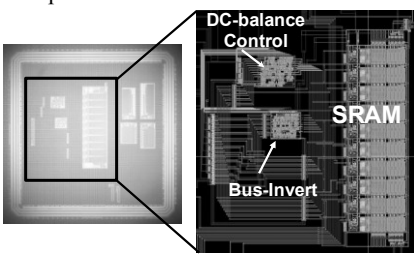
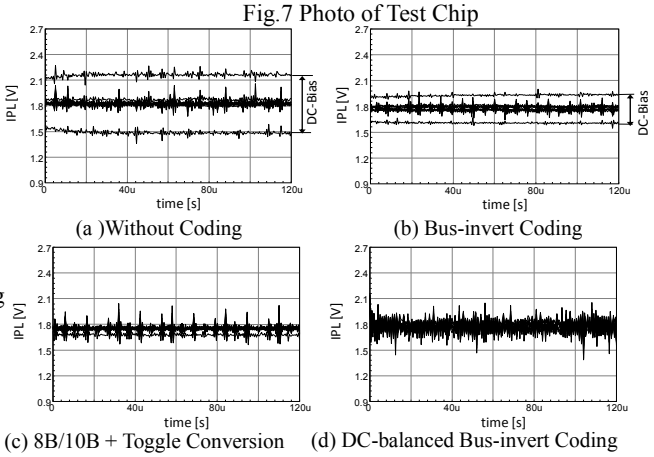


Fig.7 Photo of Test Chip



(a)Without Coding (b) Bus-invert Coding

(c) 8B/10B + Toggle Conversion (d) DC-balanced Bus-invert Coding

Fig.8 Measured Waveforms