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A Fully On-Chip Switched-Capacitor DC-DC Power Converter with Startup/Fail-Safe Circuit

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Abstract

We present a fully on-chip switched capacitor DC-DC power converter circuit that converts 3.0-V input into 1.2-V output. The circuit consists of a nano-watt reference circuit, a startup/fail-safe circuit, a pulse frequency modulation (PFM) control circuit, and a switched-capacitor circuit. Measurement results demonstrated that the circuit can convert 3.0-V input into 1.2-V output successfully. The startup and fail-safe operations were confirmed though the measurement. The efficiency was more than 50% in the range of 2–6 μA load current.

1. Introduction

Low-power and low-energy circuit designs using multiple supply voltages have been widely adopted in modern LSI systems. A DC-DC converter is one of the most important building blocks in such systems to generate appropriate supply voltages for each circuit. We present here a fully on-chip switched-capacitor DC-DC power converter circuit that converts 3.0-V input into 1.2-V output.

Lithium-based batteries are widely used as energy sources in many electronics applications. However, their nominal voltages are high (e.g., 3.0 V) and LSIs directly powered by these batteries dissipate large power. Thus, voltage scaling techniques have been widely used to achieve low power dissipation.

As an on-chip power supply circuit, switched-capacitor (SC) DC-DC converters are widely used for light load current applications [1-2]. Because MOS-transistor switches and capacitors can be easily fabricated on a silicon chip, we can develop the converter without using off-chip components. Although several converters have been reported in the previous works, we could not evaluate the circuit performance precisely because control signals such as clock signals and reference voltages/currents were supplied from off-chip instruments. Moreover, the discussion on startup and fail-safe operations were not addressed enough.

In light of this background, we present a fully integrated SC DC-DC power converter circuit. All of the circuit blocks are implemented in a chip. Details are described in the following.

2. Proposed SC DC-DC converter

Figure 1 shows our proposed SC DC-DC power converter. The converter consists of a nano-watt reference circuit [3], a startup/fail-safe circuit, a pulse frequency modulation (PFM) control circuit, and complementary SC circuits [4]. In this design, the circuit converts 3.0-V input into 1.2-V output. Thus, we set conversion ratio of the SC circuit to two-fifths (i.e., $V_{OUT} = 2/5 \times V_{IN}$). The reference circuit generates two voltages of V_{REF1} and V_{REF2} (V_{REF1} = 0.49 V and V_{REF2} = 1.1 V in this design) from the bandgap voltage reference circuit [3]. The startup/fail-safe circuit is composed of a comparator, a ring-oscillator, and a non-overlap clock generator. The PFM control circuit is composed of a comparator, a toggle flip-flop (TFF), a level shifter (LS) circuit [5], and a non-overlap clock generator. In the PFM control circuit, V_{OUT} is used as a supply voltage to reduce the power dissipation and thus the LS circuit is used to correctly switch MOS transistors. Details of the circuit operation are as follows.

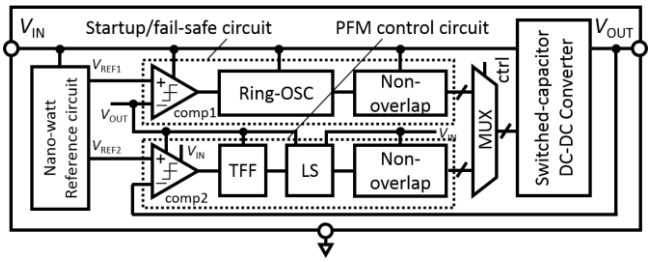

Fig. 1 Block diagram of our proposed SC DC-DC converter.

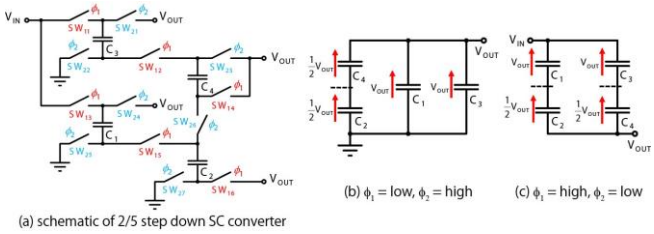

Fig.2 (a) Schematic of 2/5 SC converter and its operation: (b) ϕ_1 = low, ϕ_2 = high and (c) ϕ_1 = high, ϕ_2 = low.

When the output voltage V_{OUT} is lower than V_{REF1}, the startup/fail-safe circuit detects it and generates a clock from a ring-oscillator. The clock phase is modified adequately by a non-overlap clock generator and the clock is applied to the SC circuit. After the SC circuit generates an output voltage higher than V_{REF2}, the startup/fail-safe circuit stops the operation and the PFM control circuit takes over the control operation for high efficient conversion. When load current increases suddenly, the output voltage controlled by the PFM control circuit will go out of control. The startup/fail-safe circuit will also detect it and operate again to make the output higher than V_{REF2}.

In this work, we use 2/5 step down SC DC-DC con-

verter to convert 3.0-V input into 1.2-V output. Figure 2 (a) shows a schematic of the SC converter. The circuit consists of switches (SW_{11} – SW_{16}, SW_{21} – SW_{27}) and capacitors (C_1 – C_4). By using clock signals of ϕ_1 and ϕ_2, the connection of the capacitors are changed periodically as shown in Figs. 2 (b) and 2 (c). When ϕ_1 is low, the capacitors are connected to V_{OUT} as shown in Fig. 2 (b). Then, when ϕ_1 is high, the capacitors are rearranged as shown in Fig. 2 (b). By repeating these two configurations, the output voltage becomes two-fifths of V_{IN} ($V_{OUT} = 2/5 \times V_{IN}$).

3. Experimental Results

We fabricated a prototype chip of our proposed SC DC-DC converter using a 0.13-µm, 1P5M CMOS process technology. Figure 3 shows a micrograph of the chip. The areas was 1.62 mm^2. The capacitors of C_1-C_4 were set to 100 pF using MIM capacitor. The output load capacitor C_{OUT} (not shown in Fig. 2) was set to 200 pF using MOS capacitor. The reference voltages of V_{REF1} and V_{REF2} were designed to be 0.49 and 1.1 V, respectively, and the bias currents for the comparators were designed to be 30 nA.

Figure 4 (a) shows measured startup waveforms of our converter. The V_{OUT} increased and settled to 1.2 V correctly. After applying V_{IN}, the V_{OUT} firstly decreased. However, the startup circuit operated so that the V_{OUT} became higher than 1.1 V. Figure 4 (b) shows measured waveforms in the fail-safe operation. In this measurement, a discrete nMOS transistor driven by control signal of V_{CTRL} was connected to the V_{OUT} to emulate a sudden large load current. When the V_{CTRL} became high, the nMOS transistor flowed a large load current and the V_{OUT} decreased to zero. However, when the V_{CTRL} became low, the large load current stopped and the V_{OUT} increased again. Thus we confirmed the stable startup and fail-safe operations.

Figure 5 shows power conversion efficiency as a function of load current. The efficiency increased as the load current increased. The efficiency was more than 50% in the range of 2–6 µA. However, the operation stopped at 6 µA. The reason for this could be a design of the comparator (comp2 in Fig. 1). In this design, we used an adaptive biasing comparator to achieve both low power and high speed operation [6]. However, the adaptive bias current could not generate correctly. Therefore, the comparator could not catch up the fast operation and stopped the operation. We are now developing the modified comparator to achieve wide load current.

4. Conclusion

In this work, we designed a fully integrated switched capacitor DC-DC power converter. The circuit consists of a nano-watt reference circuit, a startup/fail-safe circuit, a PFM control circuit, and a SC circuit. Measurement results demonstrated that the proposed circuit can convert a 3.0-V input into a 1.2-V output successfully. We also confirmed that the startup/fail-safe circuit ensures the stable and robust operation of the converter.

Acknowledgements

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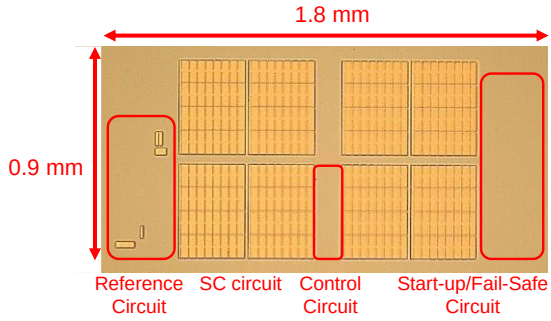
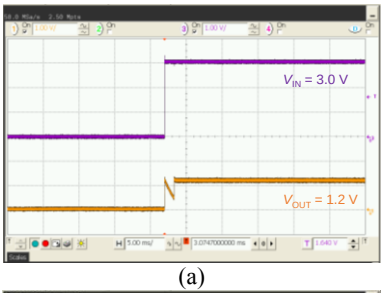
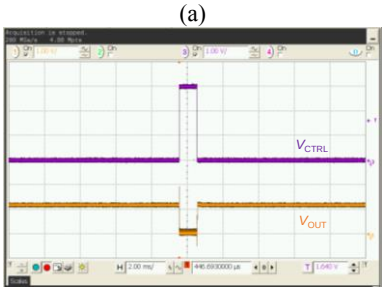


Fig. 3 Chip micrograph of proposed power converter.



(a)



(b)

Fig. 4 Measured waveforms. (a) Startup and (b) fail-safe operation.

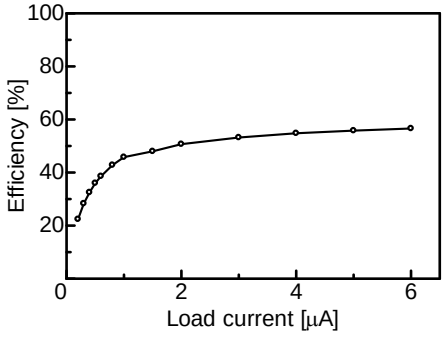


Fig. 5 Power conversion efficiency as a function of load current.