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Accuracy of Recessed Gate for GaN Power FETs and High Temperature Capability of Diamond Heat Sink

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Abstract

800V recessed gate GaN power FETs have been fabricated by using high accuracy lithography. Low on resistance less than 15 mΩ·cm^2 with high threshold voltage can be achieved with AlGaN/GaN heterostructure optimized with Al composition and thickness of step graded AlGaN layer. For the high temperature capability, diamond thin films are deposited on the back side of Si substrate. As a result, the device temperature is quickly dropped from 125 to 65 ^{o}C as increasing the thickness of nano-crystalline diamond thin film up to 0.8 μm.

1. Introduction

Recently, more efficient and improved technology of GaN power devices have been focused on automobile, smart Grid, and Industrial application to replace the conventional Si and SiC power devices because GaN has inherent advantages of high speed electron mobility, large band gap, excellent thermal stability, as well as high power capability. But, still GaN epitaxial growth should be improved with buffer layer, and the innovations of device structures are also essential for the commercialization of GaN power devices. In this work, high quality GaN epitaxial growth can be achieved with step graded AlGaN buffer layer and a new device structure is suggested by depositing diamond thin films on the back side of Si substrate, which is capable of dissipating higher temperature very fast and it is very attractive for the application of GaN power devices at high temperature environment. Furthermore, diamond thin film itself can be used for alternative high power devices. Fabrication process and electrical characteristics of normally off GaN high electron mobility transistors as well as the diamond thin films are investigated and the influence of diamond film on heat dissipation phenomena of GaN power FET has been also discussed

2. Results and Discussion

High quality epitaxial growth technology is important for high electron mobility and carrier density. When growing GaN on the Si, following points are concerned 1) large lattice mismatch between GaN and Si, 2) density of dislocation, 3) large difference of thermal expansion coefficient between GaN and Si, and 4) large stress was generated during the cool-down step. Thus, specially designed buffer layers are essential to reduce dislocation density, stress and prevent melt-back etching to achieve high quality GaN layer grown on the Si wafer. In this work, the epitaxial GaN is growth on the high temperature (HT)-AlN and step-graded AlGaN buffer layers. The growth temperature and the thickness of HT-AlN are optimized at 1100 ^{o}C and 150~180 nm, respectively. Next, the 5 step-graded AlGaN layers consist of 73 / 47 / 34 / 21 / 10 at. % of Al composition in each step and the Al concentration has been measured with AES. On these buffer layers, the high quality GaN epitaxial layer is successfully grown. Normally off GaN high electron mobility transistor with a higher gate threshold voltage leaves enough margins for operation safety and noises. High V_T of 3.5 V can be obtained with recessing the gate region and V_T strongly depends on accurate control of recess etching depth since the etched surface becomes extremely close to the 2DEG channel[1-2]. Therefore, it is very important to keep the interface no damaged by the recessed gate process and to control etch depth and uniformity, which leads to relatively low R_{on} of 15 mΩ·cm^2. The recessed gate process has been done with 300W RF and DC bias, and the chemical formations are BCl_3 and Cl_2. The variation of recessed depth vs BCl_3/ (BCl_3 + Cl_2) has been found with changing DC bias and flow rate of chemical formations and recessing time. In this process, we have recessed 26.6nm AlGaN and etch stop on the 2D channel. Since the recessed process leads to surface damage & roughness, which influences on mobility degradation, leakage current, and Interface charge/charge trapping in gate insulator, which leads to V_T drift, it is important to eliminate these problems related with recessed process[2]. In this work, we have developed a new method using a tetramethylammonium hydroxide (TMAH) treatment to eliminate these problems during the recessed process. The TMAH treatment carries on with wet etching to remove the plasma damage introduced during the recessed process and smoothening of the recessed surface. After the recessed gate structure we have determined the recessed gate profile

with AFM. And, the gate leakage current and Poole-Frenkel emission have been measured with trap-assisted tunneling on the recessed gate with and without the TMAH treatment. Then, it is found that the leakage current is extremely reduced by the TMAH treatment. The gate leakage is 2.6 x 10^{-11} A/mm at V_G of -10V, which is extremely lower than the case of gate structure without the TMAH treatment where the leakage current is 2.3 × 10^{-7} A/mm at the same gate voltage. A key issue of GaN HEMT is breakdown voltage since automobile or industry power switching converter should manage 600~1000V. In this work, we have developed the field plate to reduce the gate edge electric field and maximize the breakdown voltage. Another important point is to suppress the collapse phenomena. It is done by minimizing the gate-edge electric field since the field plate offers an additional edge for the E-field lines to terminate and reduce the gate edge electric field, lowering electron injection into traps. Finally, diamond thin films are deposited on the back side of Si substrate. Normally, diamond thin films are unable to be deposited on Si surface. So, high frequency plasma is applied to parallel pate in the CVD chamber using CH_4-H_2 gas, and the growth rate is 1.5 μm/hr.

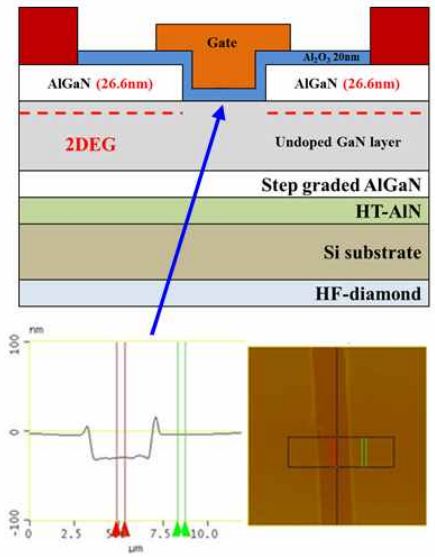

Fig. 1 Structure of GaN HEMT and profile of recessed gate

As a result, the electric field is reduced by 40% at the optimum extended field plate of 20 μm and the maximum breakdown voltage is 830V as shown in Fig. 2.

During the operation of GaN HEMT, surface temperature on the GaN device is measured with and without the diamond heat sink. Fig. 3 shows that the surface temperature abruptly decreases from 125 to 65 °C as increasing the thickness of diamond film up to 0.8 μm. This means that the joule heat generated by the operation of high power device is effectively dissipated with thicker diamond thin film used as the heat sink.

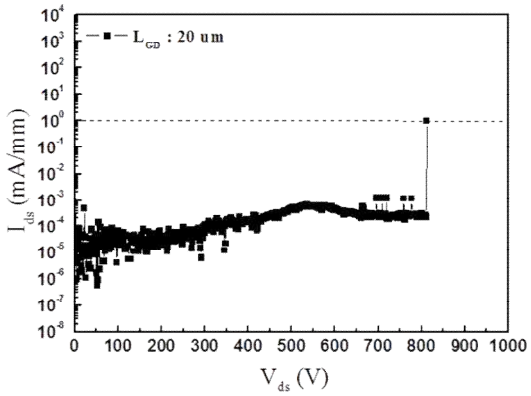

Fig. 2 Breakdown voltage of GaN HEMT

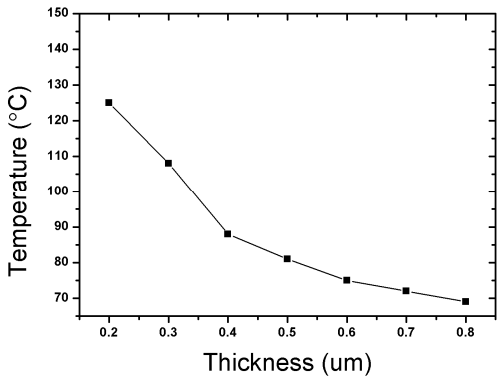

Fig. 3 Temperature of GaN power device during the high power operation vs thickness of diamond thin film as heat sink

3. Conclusions

GaN HEMT has been fabricated with the recessed gate and the diamond thin film is deposited on the back side of Si substrate as the heat sink. For the GaN HEMT, high quality epitaxial growth of GaN can be achieved with the high temperature AlN and 5 step graded AlGaN buffer layers. Damage free recessed gate is successfully done with optimum etching condition and TMAH treatment. Using the extended field plate the electric field can be reduced by 40% and the breakdown voltage is 830 V. Diamond thin films are deposited on the back side of Si substrate to dissipate heat from the devices. As a result, it is found that the diamond heat sink is very effective to reduce the operation temperature, and the thicker diamond films the lower temperature can be obtained.

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