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Study on Electrical Performances of ZnO-TFTs with 3-D Finlike Channels Fabricated by Nanoimprint Lithography and Atomic Layer Deposition

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Abstract

This study focuses on the electrical performances of ZnO TFTs with 3-D finlike channels fabricated by nanoimprint lithography (NIL) and atomic layer deposition (ALD). The 3-D finlike structures were fabricated by NIL; the ZnO active layers were deposited by ALD and following by suitable annealing conditions. The 3-D finlike TFTs show higher mobility (>6 cm^2/Vs), lower threshold voltage, and smaller subthreshold swing than that with single channels.

1. Introduction

Recently, the oxide-TFTs have been studied for novel active-matrix displays (AMDs) applications, such as smart phone, tablet, and large size TVs [1-2]. High performances and stability oxide-TFTs have been reported [3]. Besides, the TFTs with 3-D finlike structure were also proposed [4].

In this paper, the ZnO active layers were deposited by ALD following by the low temperature annealing in air, O_2, or Ar ambient. Besides, 3-D finlike channels were used to improve the performance of the ZnO TFTs. The performance of proposed TFTs were studied and compared to the single ones.

2. Device Fabrication

The oxide TFTs with single and 3-D finlike structure of fabricated by nanoimprint lithography (NIL) have been shown in Fig. 1 (a) and (b). The Si mold, used in nanoimprint lithography, with two kinds of nanoscale line width/space about ~200/200 and 200/400 nm, was fabricated with E-beam lithography and reactive ion etching (RIE). Then, the 3-D finlike patterns, with an alignment key for conventional lithography, were imprinted by the thermal-NIL technique with PMMA resist at an imprinting pressure of 300–500 psi. O_2 plasma was applied to remove the residual layer of NIL, and then the 3-D finlike structures were fabricated by reactive-ion etching (RIE) in CF_4 for 1–3 min. Next, the stacked oxide layer, 10-nm-thick tetraethylorthosilicate (TEOS) oxide deposited by LPCVD and the 30-nm-thick HfO_2 deposited by atomic layer deposition (ALD), was used. A 50-nm, ZnO film as a active layer was deposited on the dielectric surface by ALD at substrate temperature 100°C, and then following by the low temperature annealing at 250°C.

In this work, four kinds of ZnO film low temperature annealing were studied. They are denoted by A (Ar, Ar annealing in chamber), B (Ar+HP, Ar annealing in chamber and then hotplate in the air), C (O_2, O_2 annealing in chamber), and D (O_2+HP, O_2 annealing in chamber and then hotplate in the air). The Al film were also selected as the source and drain electrodes and the channel length and width of ZnO TFTs are 20 and 200 μm, respectively. Finally, the 300/100 nm-SiO_x/SiN_x film as a passivation layer was deposited by PECVD.

3. Results and Discussion

Figure 2 demonstrates the transfer characteristics and mobility curve of the device with A, B, C, and D annealing condition. The electrical parameters of TFTs, such as the Vt, subthreshold slope (SS), and mobility, can be acquired from the conventional metal oxide semiconductor field effect transistor (MOSFET) equation. The drain-source voltage (V_{DS}) were fixed at 1 V and the gate-source voltage (V_{GS}) varied from -5 ~ 20 V. The device D (O_2+HP) exhibited high performances, including high on/off ratio, low Vt, small SS, and high mobility, as compared with device A, device B and device C. The results could be attributed that the oxygen annealing in the chamber and the additional hotplate annealing in the air may effectively suppress the oxygen vacancy and thermal-induced oxygen atoms which move from the initial site to interstitial site in the ZnO thin films.

Figure 3 illustrates the output characteristics of the device with four kinds annealing condition when the drain-source voltage (VDS) swung from 0 ~10 V and the gate-source voltage (VGS) varied from 0 ~ 12 V step 3V. The high output drain current and obvious square law behavior of device D were better than that of those with other annealing conditions. The results could be attributed to high grain size and obvious crystal size. In contrary, the device A exhibited the abnormal output curve that is due to the high oxygen vacancies in the ZnO thin film.

Figure 4 compares the electrical characteristics of the devices D with the single channel and 3-D finlike channels, respectively. The 3-D finlike ZnO TFTs with the line width/space of about ~200/200 nm show the lower Vt, the small SS, and higher on/off ratio than that with the single channel. Moreover, the ZnO TFTs, with 3-D finlike channels of line width/space values about ~200/200 nm, have high mobility as compared with others. The results show that the 3-D finlike ZnO TFTs, with the line width/space of about ~200/200nm, have optimal device performance.

4. Conclusions

In summary, in this paper, performance of ALD ZnO film based TFTs with the single and 3-D channels were studied, respectively. The highly performances of 3-D channel ZnO TFTs with suitable annealing condition were demonstrated. The TFTs exhibited improved mobility, SS and Vt of about ~6.5 cm^2/Vs, ~0.7 V/dec, and 0.1 V. This process can be used for the future display applications.

Reference

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Figures

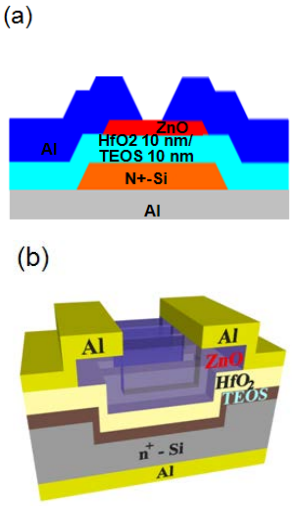

Fig. 1 The structure of ZnO thin film transistors with (a) single channel, (b) 3D channel are the bottom gate and top contact.

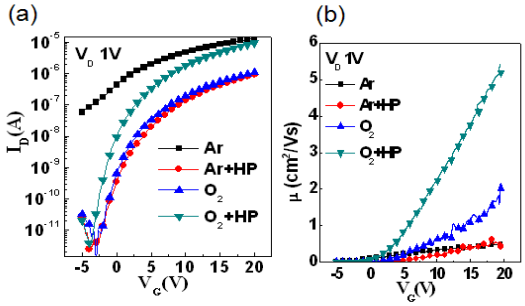

Fig. 2 (Color online) The electrical (a) transfer curve and (b) mobility characteristic of ZnO TFT with four kinds annealing condition.

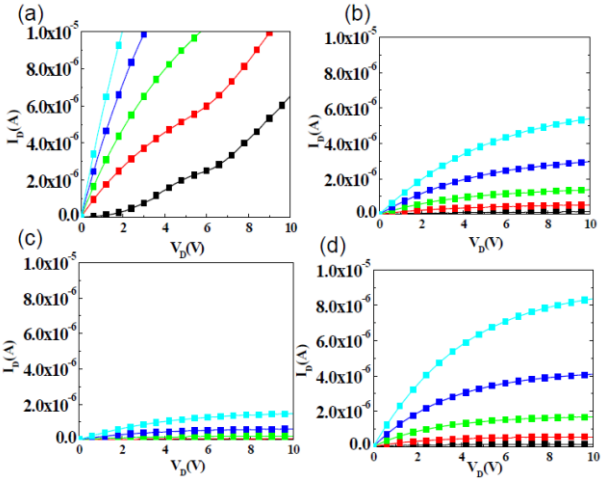

Fig. 3 (Color online) The output characteristic of device with the annealing condition of (a) Ar, (b) Ar+HP, (c) O_2, and (d) O_2+HP.

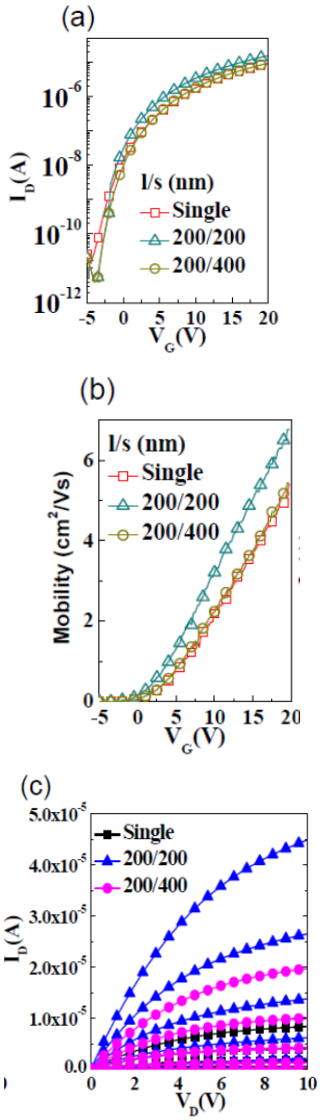

Fig. 4 (Color online) The electrical characteristics (a) transfer curves, (b) mobility characteristics, and (c) output curves of ZnO TFTs with Single and 3D channels.