Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp210-211

Impact of Gate Dielectrics and Oxygen Annealing on Tin-Oxide Thin-Film Transistors

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Abstract

This work reports the evolution of transfer characteristics of tin-oxide TFTs with annealing performed in oxygen ambience. From the results of Hall measurements and *I-V* characterization, we confirm that the properties of the channel films transform from an *n*-type tin-rich phase to an intermediate resistive state, and then to the *p*-type SnO phase. Impacts of the gate dielectrics in SnO TFTs on the transformation process are also revealed.

1. Introduction

SnO has been pointed out as a promising oxide semiconductor for p-type TFTs [1]-[2], understandings about the effects of the underlying gate dielectric and annealing treatment are still insufficient. In this work, we show for the first time clear evidences about the transformation of thin film structure with annealing period in oxygen ambience and its impact on the device performance. The effects of the underlying dielectric on the crystallization are also explored.

2. Device Fabrication

Fig. 1 shows the conventional bottom-gated architecture adopted in this work for fabricating *p*-type SnO TFTs. We started the fabrication on a silicon substrate capped with a 300 nm-thick SiO_2. The bottom gate is 200 nm-thick Al and 20nm-thick three types of gate dielectrics, namely, SiO_2, HfO_2, and Al_2O_3 were employed. A 15 nm-thick tin-rich oxide channel layer was deposited by sputter. A 100 nm-thick Ni film was deposited by an e-gun evaporator and lift-off process to form S/D pads. After the device fabrication, the annealing process was done in furnace in an oxygen ambience (0.3 torr and 15 sccm O_2) at 300°C.

3. Results and Discussion

Fig. 2 shows the evolution of transfer characteristics with increasing cumulative anneal (CA) time obtained from a device with SiO_2 gate oxide. In this experiment the annealing was interrupted several times by pulling out the wafers for device measurements, so the annealing time specified in the figure is"cumulative". In the figure, the I-V curve is initially not able to be modulated (1st stage) by the gate bias owing to the high electron concentration. From the Hall measurements, the as-fabricated film is tin-rich, metallic and *n*-type with a high electron concentration (> 10^{19} cm^{-3}). Interestingly, the drain current is significantly dropped (2nd stage) with CA time of 15 minutes, owing in part to the oxidation of the tin-rich film which tends to reduce the electron concentration. When CA time is increased to 30 minutes, the film would be dominated by the SnO phase and, therefore, the device shows *p*-type characteristics (3rd stage). Similar phenomena are also observed on the devices with HfO_2 and Al_2O_3 gate dielectrics, although hindrances to the final transformation to *p*-type operation are found. The three stages in the evolution for various splits of devices are illustrated in Fig. 3 in which the current at V_G = -3 V is shown as a function of the CA time.

During the study, we also found that the images of optical microscope (OM) taken on the devices can be used to monitor the crystallization status, as the color of the channel film changes from dark (Fig. 4(a)) to bright (Fig. 4(b)). Corresponding XRD results are shown below the OM images. Figure 5 shows OM images of the three splits of devices with CA time of 30 minutes (the data encircled in Fig.3). Obviously it reveals that the crystallization of the tin-oxide layer is affected by the underneath gate dielectric. Fig. 6(a) shows the transfer characteristics of *p*-type SnO TFTs with various gate dielectrics after a sufficient annealing treatment. Fig. 6(b) shows well-behaved output characteristics of an SnO TFT. Field-effect mobility values of the SnO TFTs are extracted and compared with the best results ever reported on devices with planar structures in the literature [2]-[4] in Table 1.

4. Conclusions

In this work, an interesting evolution of transfer characteristics of the devices having various gate dielectrics with oxygen annealing is observed and the trends are consistent with the changes in the micro-structure of the tin-oxide layer. We've also shown that the OM images can be used to check the crystallization status of the tin-oxide layer. With a sufficiently long treatment, SnO TFTs with good device performance can be obtained.

Acknowledgments-This work was sponsored in part by the Ministry of Science and Technology, Taiwan, under Grant-NSC-102-2221-E-009-097-MY3, and NCTU-UCB I-RiCE program, under Grant MOST-104-2911-I-009-301, and the Ministry of Education of Taiwan under ATU Program.

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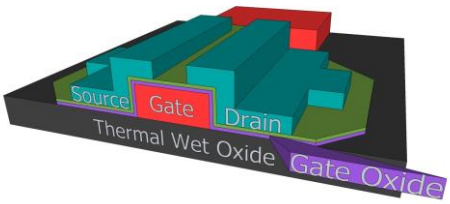

Fig. 1. The bottom-gated TFT structure employed for fabricating the test devices.

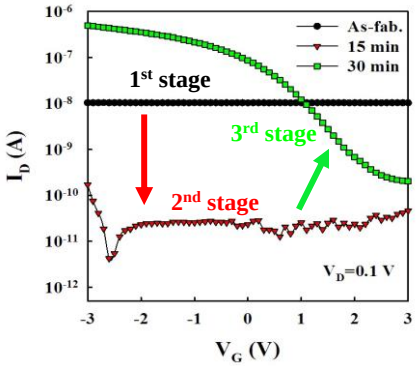

Fig. 2. Evolution of transfer characteristics with increasing CA time for a TFT with a SiO_2 gate oxide.

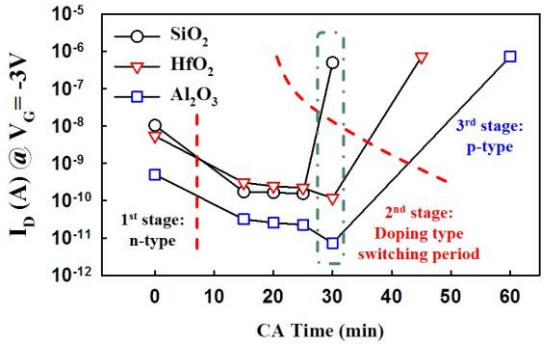

Fig. 3. Evolution of transfer characteristics with increasing CA time for TFTs having various gate dielectrics.

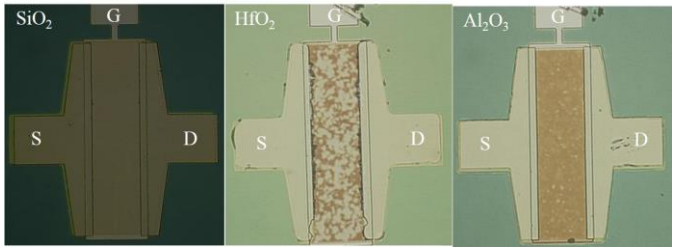

Fig. 5. OM images of the three devices characterized in Fig. 3 taken at CA time of 30 minutes.

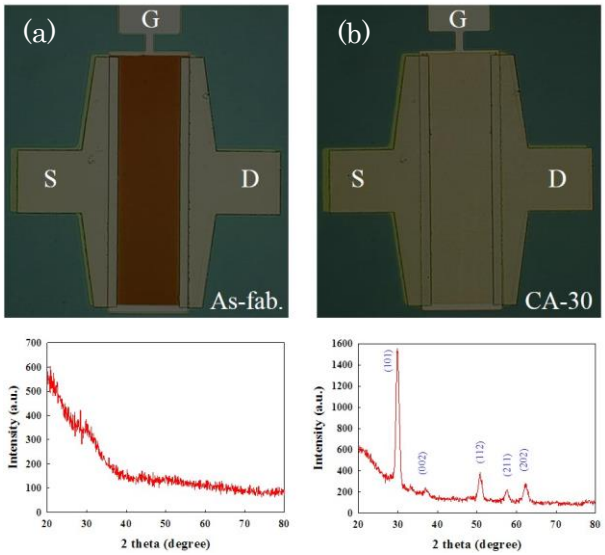

Fig. 4. OM pictures taken on a sample (a) before and (b) after going through a long annealing treatment. Corresponding XRD results are shown below, indicating that the OM images can serve as a quick check for the crystallization status of the tin oxide channel film.

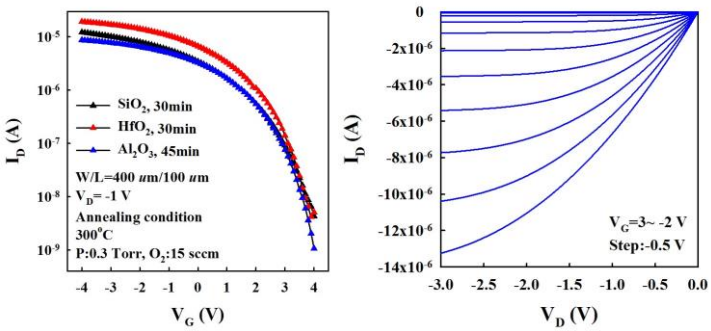

Fig. 6. (a) Transfer characteristics of SnO TFTs with various gate dielectrics and experienced sufficiently long annealing treatments. (b) Output characteristics of a SnO TFT with a SiO_2 gate dielectric.

Table 1. Comparisons of major electrical parameters for SnO TFTs having different gate dielectrics reported in this work and previous literatures.

Mobility ($cm^2V^{-1}S^{-1}$)	V_{th} (V)	I_{on}/I_{off} ratio	Gate dielectric	Ref.
6.75	0.50	$>10^3$	HfO_2	[2]
5.59	-4.81	$\sim10^2$	SiO_2	[3]
3.40	**1.88**	**$\sim10^4$**	**SiO_2**	**This work**
1.94	**2.20**	**$\sim10^4$**	**HfO_2**	**This work**
1.80	50	$\sim10^3$	SiO_2	[4]
1.77	**2.36**	**$\sim10^4$**	**Al_2O_3**	**This work**