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Design of drain for low off current in GaAsSb/InGaAs tunnel FETs

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Abstract

The impact of drain design in a GaAsSb/InGaAs double gate vertical tunnel FET is simulated. The design of drain is effective in suppressing off current in TFET and it can be decreased by reduction of drain doping concentration. However, due to access resistance in drain, on-current reduction is also confirmed. When we introduce wider bandgap in drain with step-graded layer, reduction of off current is also confirmed without degradation of on-current.

1. Introduction

To obtain steep subthreshold slope in FETs for low-power application, tunnel FETs are attractive candidate[1]. One of the drawback of tunnel FETs is lower on-current due to tunnel resistance. To reduce tunnel resistance, introduction of narrow bandgap material and staggered (type-II) heterojunction are effective [2,3]. In our former report [3], impact of source doping concentration was reported. However, to our knowledge, design of drain has not been reported in tunnel FET with staggered hetero-junction.

In this work, we study the off current`s dependence on doping concentration and drain/channel In fraction in a GaAsSb/InGaAs tunnel FET through simulation.

2. Doping concentration dependence

The simulation structure is shown in Fig. 1. The double gate structure is assumed from our experimental structure [3]. The model has a 40-nm-thick p^+ $GaAs_{0.51}Sb_{0.49}$ region (8×10^{19} cm^{-3}) as the source, a 40-nm-thick undoped $In_{0.53}Ga_{0.47}As$ region (5×10^{15} cm^{-3}) as the channel, and a 40-nm-thick n^+ $In_{0.53}Ga_{0.47}As$ region as the drain. The InGaAs and GaAsSb composition is chosen as the lattice-matched composition on the InP substrate. The body width (*y*-direction, as shown in Fig. 1) is assumed to be 10 nm. Because we select SiO_2 as the insulator, the insulator thickness is equal to the effective oxide thickness (EOT) of 1 nm. The Silvaco Atlas simulator with a non-local tunneling model is used for the calculation. Fig.2 shows simulated I-V characteristics. Off point of Fig. 2(a) is determined by intersection of tunneling current from source to channel (hole to electron) and that from drain to channel (electron to hole). Thus reduction of doping concentration of n-InGaAs drain region is effective to reduce off point. However, when we reduce doping concentration, reduction of on-current is confirmed as shown in Fig. 2(b). This is due to increase of series resistance in the drain when large on-current flows. At present, on-current is defined when gate bias is sum of supplied voltage and gate bias corresponding the off-current. If we assume 10 pA/μm as off-current and 0.5 V as power supply, on-current is estimated as 466 μA/μm when drain doping concentration is 8×10^{18} cm^{-3}.

a)

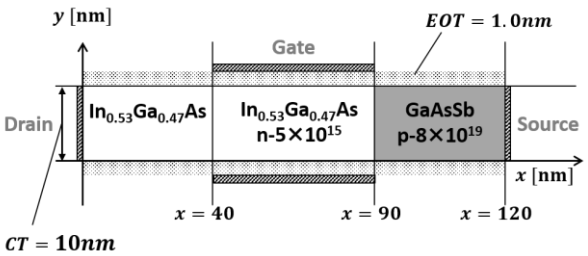
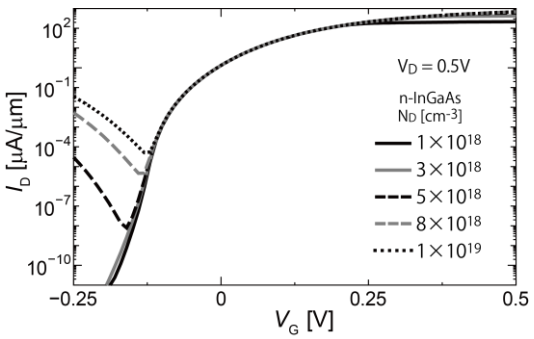


Fig. 1 Simulation structure of the tunnel FET for doping concentration dependence.

a)



b)

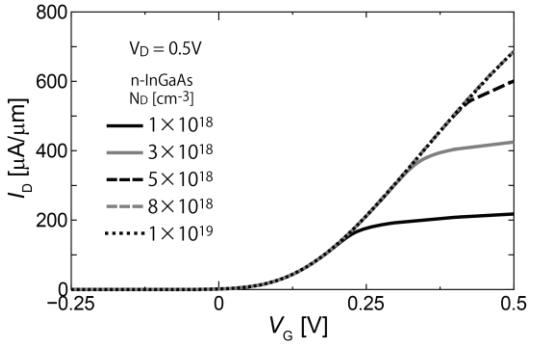


Fig. 2 Simulated I-V characteristic for different doping concentration of drain. a) Log-scale plot and b)linear-scale plot.

3. Composition dependence

Because off current is determined by tunneling from drain to channel, composition change of drain is also effective to reduce off current. Fig. 3 shows the structure to change the composition of drain. In model (a), Indium composition of drain is changed from 0.53 to 0.4. The other conditions are kept constant. Because abrupt composition change has possibility to suppress on-current, 3-nm thick step graded layer with indium composition of 0.46 is introduced in model (b). Fig.4 shows simulated I-V characteristics. I-V characteristics obtained in Fig.2 for the doping concentration of 8×10^{18} cm^{-3} has been shown in Fig. 4 for reference. By using wide bandgap material, tunneling from drain to channel is suppressed as shown in Fig.4 (a). However, from Fig.4 (b), clear degradation of on-current is confirmed when we use abrupt junction. When we use step-graded layer, obtained on-current is almost equal to the reference.

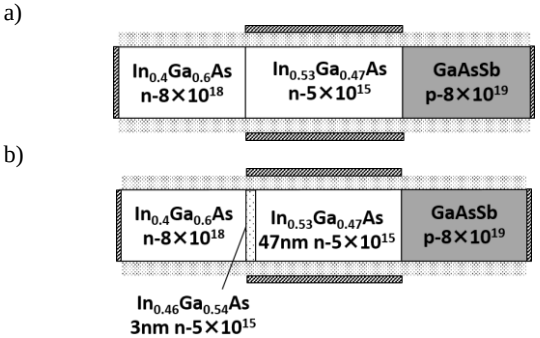


Fig. 3 Simulation structure of the tunnel FET for composition dependence. a) Abrupt junction. b) With step-graded layer.

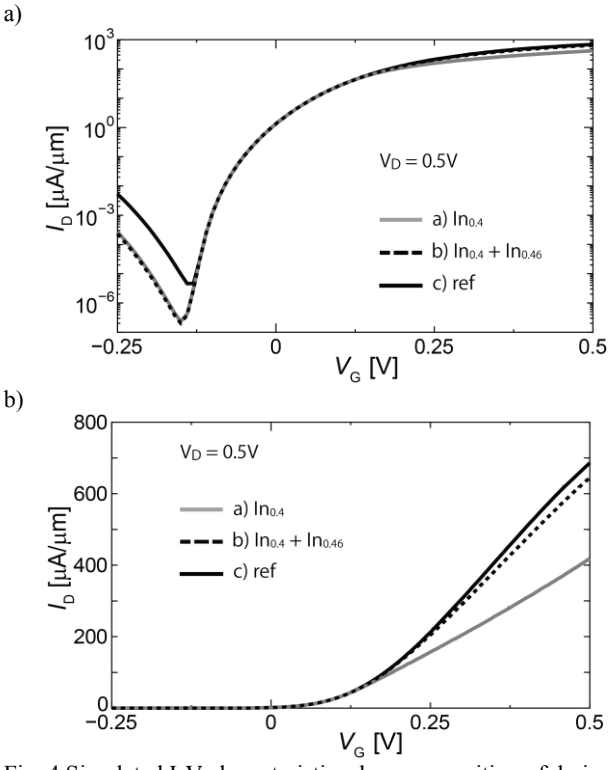


Fig. 4 Simulated I-V characteristic when composition of drain was changed. a) Log-scale plot and b)linear-scale plot. Reference is I-V curve in Fig.2 at the doping concentration of 8×10^{18} cm^{-3}**.**

Fig. 5 shows band-profiles when gate bias was -0.2 V. As shown in arrow in the figure, tunneling current from drain to channel passes through wide-bandgap region, results in lower off current.

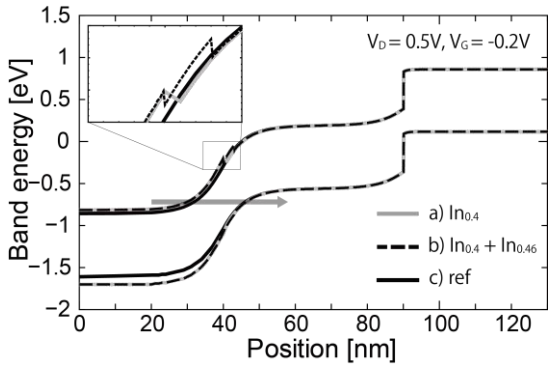


Fig. 5 Calculated band profiled of the tunnel FET for composition dependence.

If we assume 1 pA /μm as off-current and 0.5 V as power supply, on-current is estimated as 410 μA/μm when step-graded layer is used.

Because channel length of tunnel FET is determined by intersection of tunneling current from source and that from drain, presented reduction of off current has the possibility to reduce channel length, i.e., reduce gate capacitance.

3. Conclusions

We calculated drain structure dependence of the double gate tunnel FET with GaAsSb/InGaAs staggered hetero-junction. When drain doping concentration is reduced, off current can be reduced. However, on-current is also reduced due to access resistance. When we introduce wider bandgap in drain with step-graded layer, reduction of off current is also confirmed without degradation of on-current.

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