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Improved Linearity and Reliability in GaN MOS-HEMTs Using nanolaminate La_2O_3/SiO_2 Gate Dielectric

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Abstract—Improved device property for linear power applications has been discussed in this study. We have compared the La_2O_3/SiO_2 AlGaN/GaN MOS-HEMTs with other La_2O_3-based (La_2O_3/HfO_2, La_2O_3/CeO_2 and single La_2O_3) MOS-HEMTs. It was found that forming lanthanum silicate films can not only improve dielectric quality but also can improve device characteristics. The improved gate insulating, reliability and linearity by 8-nm La_2O_3/SiO_2 MOS-HEMT was demonstrated.

1. Introduction

GaN metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs) has been intensively investigated due to their larger voltage swing, high breakdown field and lower gate leakage current, as compared with the conventional Schottky HEMTs[1,2]. Among the dielectric materials, La_2O_3 is one of the attractive due to its high dielectric constant, large bandgap and better thermal stability[3]. However, it is chemically unstable in air by reacting with CO_2 to form $La_2(CO_3)_3$ or absorbing water to form LaO(OH) . Recently, some research have been focused on the properties of lanthanum silicate films, which was found to be much more inert with respect to hydroxide and carbonate formation, and less likely to contain oxygen deficiencies[1,4]. SiO_2 is hydrophilic and has large energy band offset with GaN, we believed that forming lanthanum silicate films can not only improve dielectric quality and stability but also can further improve device reliability, linearity and other dc property. Thus in this study, we fabricated the AlGaN/GaN MOS-HEMTs with 8 nm nano-laminate La_2O_3/SiO_2 gate dielectrics and compared with other kinds of La_2O_3-based MOS-HEMTs (La_2O_3/HfO_2, La_2O_3/CeO_2 and single La_2O_3) and Schottky-gate HEMTs. The improved linearity and reliability had been demonstrated in La_2O_3/SiO_2 MOS-HEMTs.

2. Device fabrication and measurement

The samples used in this study were grown on silicon substrate by MOCVD. It includes 1µm GaN buffer, 25nm undoped AlGaN barrier and 10nm undoped GaN cap layer. The fabrication processes started from the device isolation by ICP mesa etching using Cl_2 gases. The etching depth was 200nm. Then, the multilayer metal of Ti/Al/Ni/Au was deposited using E-Gun evaporator and annealed by rapid thermal annealing (RTA) system at 800°C for 60 sec in N_2 ambient to form Ohmic contact, and the spacing of source-drain was 20µm. Four kinds of 8 nm nanolaminate La_2O_3-based film(La_2O_3/SiO_2, La_2O_3/HfO_2, La_2O_3/CeO_2 and single La_2O_3) was deposited by molecular beam deposition (MBD) as the gate dielectric, the thickness has been checked by transmission electron microscopy (TEM). Fig.1 shows the schematic diagram of the stacked La_2O_3-based MOS-gate structure. Afterward, a post–deposition annealing (PDA) was carried out at 600°C in N_2 ambient for 5 minutes. Finally, Ni/Au gate metal was deposited by E-Gun evaporator, and the gate length used was 2µm. The conventional HEMTs were fabricated for comparison which had same process steps except for gate dielectric deposited. Agilent E5270B device analyzer was used for DC characteristic and the reliability test. Intermodulation characteristic were measured by HP8753D network analyzer.

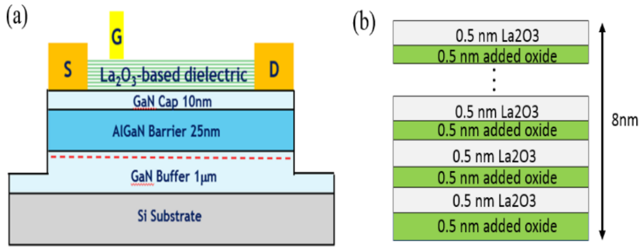

Fig.1 Schematic diagram of the (a) AlGaN/GaN MOS-HEMT (b) nano-laminate of La2O3-based gate dielectric

3. Results and discussions

3.1 DC measurements

Fig.2(a) shows the dc transfer characteristics for the studied devices, it was observed that the maximum drain current (I_{DMAX}) of La_2O_3/SiO_2 MOS-HEMTs is the highest, the improved gate insulating property was shown in Fig 2(b). The reduction of gate leakage current of La_2O_3/SiO_2 MOS-HEMTs is due to the larger bandgap of lanthanum silicate films. Table.1 shows the result of measurement. The larger gate-voltage swing (GVS), breakdown voltage (BV) and better subthreshold slope (SS) was observed in La_2O_3/SiO_2 MOS-HEMTs. However, the threshold voltage (V_{TH}) of La_2O_3/SiO_2 MOS-HEMTs was relatively negative due to its lower dielectric constant as compared with others.

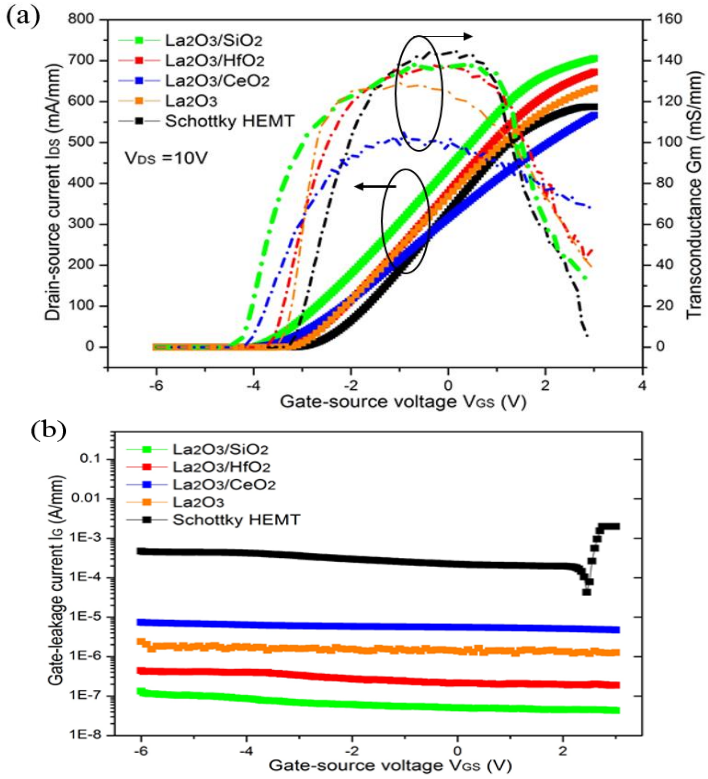

Fig.2 (a) dc transconductance, (b) I_G-V_G characteristics of the studied devices.

	La_2O_3/SiO_2	La_2O_3/HfO_2	La_2O_3/CeO_2	La_2O_3	Schottky HEMT
I_{DMAX} (mA/mm)	**705**	672	567	633	587
Gm_{MAX} (mS/mm)	**139**	138	106	130	146
V_{TH} (V)	**-4.00**	-3.45	-3.9	-3.5	-3.05
GVS (V)	**3.05**	2.75	2.3	2.8	2.15
BV (V)	**600**	470	410	425	325
SS(mV/decade)	**92**	101	140	123	260

Table.1 Comparison measured data of studied devices.

3.2 Reliability test

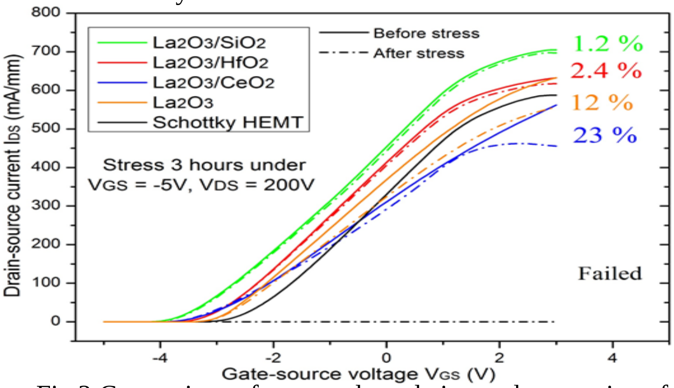

Fig.3 Comparison of current degradation and proportion after high voltage stress.

The reliability test was executed under drain-source voltage (V_{DS}) of 200V and gate-source voltage (V_{GS}) of -5V for 3 hours. Fig.3 shows La_2O_3/SiO_2 MOS-HEMTs had only 1.2 % current degradation after high voltage stress and Table.2 also shows the stability of gate capacitance, which were due to the improvement of gate dielectrics quality and gate

	Before stress		After 3 hours stress		ΔC	
	Cgd (pF/mm)	Cgs (pF/mm)	Cgd (pF/mm)	Cgs (pF/mm)	ΔCgd	ΔCgs
La_2O_3/SiO_2	0.672	11.12	0.722	11.78	**7.4%**	**5.9%**
La_2O_3/HfO_2	1.05	12.86	1.142	13.44	8.7%	4.5%
La_2O_3/CeO_2	0.674	20.6	0.81	24.6	20.2%	19.4%
Schottky HEMT	0.766	18.02	Fail	Fail		

Table.2 Comparison of stability of gate capacitance

insulting characteristics. The larger breakdown voltage and better reliability of La_2O_3/SiO_2 MOS-HEMTs showed a great potential for power applications.

3.3 Intermodulation characteristics

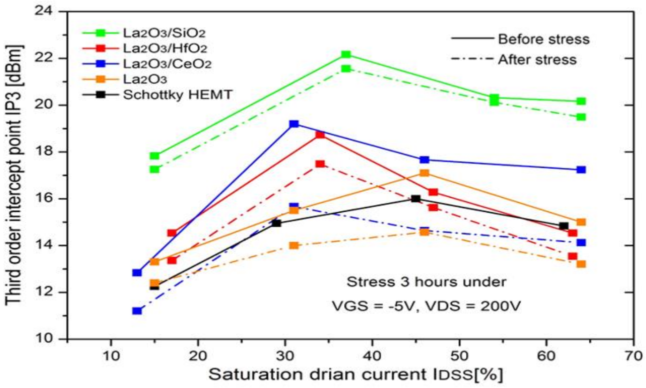

Fig.4 IP3 versus I_{DS} curves for studied device, the test frequency is 2GHz and V_{DS}=20V

Since the larger output current and wider GVS, the maximum third-order intercept (IP3) value of La_2O_3/SiO_2 MOS-HEMTs was 22.16 dBm and showed totally higher than other devices versus different I_{DS}. After 3 hours high voltage stress, La_2O_3/SiO_2 MOS-HEMTs also showed less degradation of IP3 value. The result was shown in fig.4.

4. Conclusions

The 8nm molecular beam deposited nano-laminate La_2O_3/SiO_2 MOS-HEMTs was compared with the same thickness of La_2O_3/HfO_2, La_2O_3/CeO_2 and La_2O_3 MOS-HEMTs. The improved output current, gate insulating, reliability and linearity was demonstrated in this study which showing the great potential of La_2O_3/SiO_2 MOS-HEMTs for high-linearity power applications.

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