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# Study of AlGaN/GaN Tri-gate HEMTs for Device Performance Improvement

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**Abstract**

**GaN tri-gate HEMTs with different etching depth is studied for perform comparison. The 3-D tri-gate structure has better gate controllability compared to conventional planer structure. That trigate approach reduced the short channel effects such as drain-induced barrier lowering (DIBL), and reduced the SS and $R_{ON}$, result in better switch speed.**

## 1. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are promising devices for high speed and high power applications because of the high breakdown voltage, high saturation velocity and high sheet carrier density. The large 2-D electron gas (2-DEG) at AlGaN/GaN heterointerface is essential for reducing the ON-resistance ($R_{ON}$), which is an important property to improve efficiency, heat, and power dissipation for power switch applications. To operate the transistor at higher switch speed, the common approach is to shorten the gate length (Lg). However, when the Lg is shortened, the short-channel effect (SCE) is inevitable if the top barrier thickness does not shrink as well, which increases the subthreshold swing (SS) and effects the drain-induced barrier lowering (DIBL). Therefore, the 3-D tri-gate structure, which has better electrostatic control compared to planar-type transistors, especially for the short-channel case, is used for the suppression of short channel effects. Thus, decreasing SS and $R_{ON}$, and results in better switch speed.

In the present study, we perform numerical device investigation on the effects of body height (i.e., etching depth, *h*) on the characteristics of GaN tri-gate HEMTs. The GaN tri-gate HEMTs have better gate controllability, due to 3-D nonplanar structure, which increases ON-state performance while improving the OFF-state characteristics, and results in positive shift of threshold voltage ($V_{th}$).

## 2. Device fabrication and measurement

The AlGaN/GaN structure was grown by MOCVD on the silicon substrate. It consists of a 1 µm GaN buffer, a 22 nm undoped AlGaN barrier and 3 nm undoped GaN cap layer. The fabrication process started from the device isolation by ICP mesa etching using $Cl_2$ gases. The etching depth of mesa etching was 200nm. Then, the multilayer metal of Ti/Al/Ni/Au was deposited using E-Gun evaporator and annealed by rapid thermal annealing (RTA) system at 800°C for 60 sec in $N_2$ ambient to form Ohmic contact, and the spacing of source-drain was 3µm. The fin-shaped active region of the device, with various body height h of 125nm and 200nm, and body width of 5µm, as defined by electron-beam lithography. The separation between two adjacent bodies d is 100nm. Finally, Ni/Au gate metal was deposited by E-Gun evaporator after the gate region was defined. The gate length was 0.4 µm, the structure of the device is shown in Figure 1. Agilent E5270B power device analyzer was used for DC characteristic measurement.

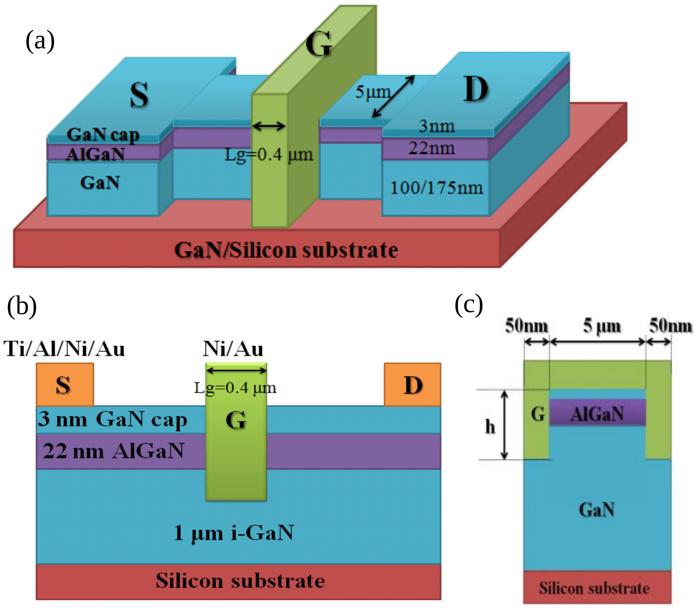


Fig. 1. (a)Schematic illustration of AlGaN/GaN tri-gate HEMT structure. (b)Front view (c) Side view

## 3. Results and discussions

3.1 DC characteristics

In Figure 2(a), the tri-gate GaN HEMTs shows significant improvement in ON resistance ($R_{ON}$) as compared to planer HEMT. The $R_{ON}$ of devices with the body height (*h*) of 125nm and 200nm are 3.17Ω/mm and 4.13Ω/mm respectively, which is 5.12Ω/mm for planer HEMT. Figure 2(b) shows that threshold voltage ($V_{th}$) shifts towards positive from -4.82V for planer to -3.68 and -3.56 for devices with h of 125nm and 200nm respectively. The maximum transconductance (gm) are 170mS/mm, 197mS/mm and 193mS/mm for planer, h of 125nm and 200nm, respectively.

The maximum drain-source current for planer is 993mA/mm, which are 920mA/mm and 830mA/mm for h of 125nm and 200nm.

The subthreshold swing (SS) in figure 3(a) exhibits remarkable progress from 398 mV/decade for planer, 82mV/decade for etching depth of 125nm and 75 mV/decade for etching depth of 200nm. Both devices show negligible drain-induced barrier lowering (DIBL), the DIBL of etching depth of 125nm shows in Figure 3(b). Figure 4 shows breakdown voltage of 123V for etching depth of 125nm device.

3.2 Etching depth effect

The etching depth of 200nm device shows slightly lower SS and positive shifts of threshold voltage. However, the etching depth of 125nm one shows much lower $R_{ON}$, higher $I_{DMAX}$ and higher breakdown voltage as shown in table below.

| Etching depth | Planer | 125nm | 200nm |
|---|---|---|---|
| $I_{DMAX}$(mA/mm) | 993 | 920 | 830 |
| $G_{MMAX}$(mS/mm) | 170 | 197 | 193 |
| $V_{th}$(V) | -4.82 | -3.68 | -3.56 |
| $R_{ON}$(Ω/mm) | 5.12 | 3.17 | 4.13 |
| SS(mV/decade) | 398 | 82 | 75 |
| $I_{ON}/I_{OFF}$ | $5.57\times10^{1}$ | $3.42\times10^{4}$ | $1.02\times10^{5}$ |

Table. Comparion of DC characteristics of device of different etching depth.

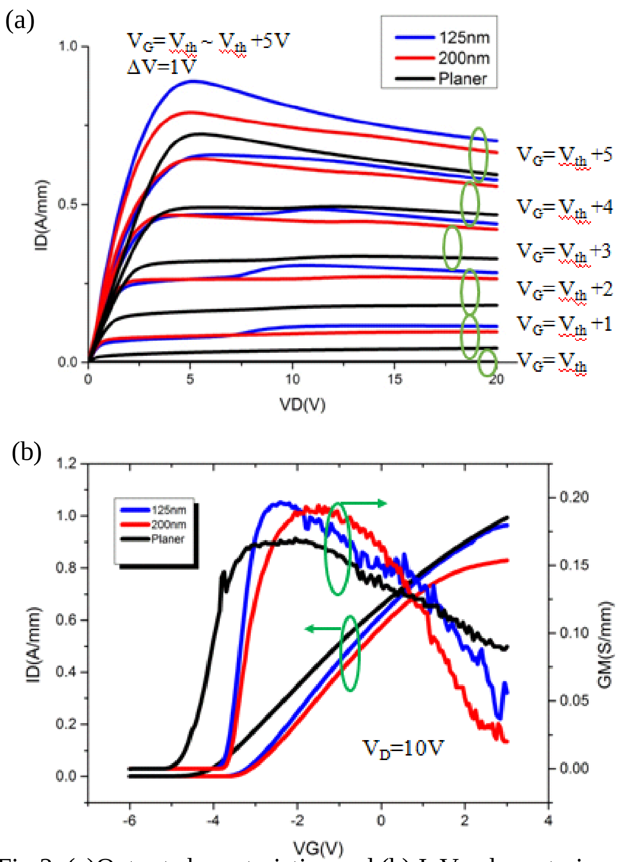


Fig.2. (a)Output characteristics and (b) $I_D V_G$ characteristics of the GaN tri-gate HEMTs.

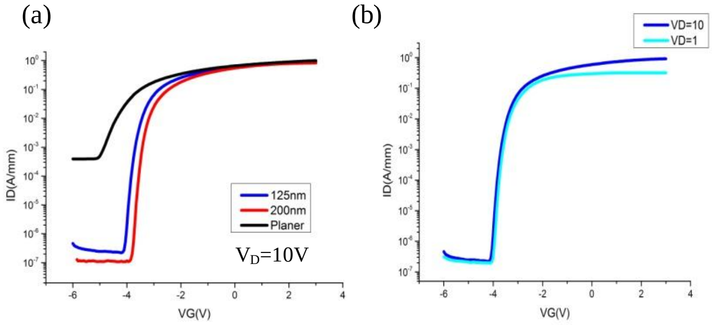


Fig.3. Log($I_D$)-$V_G$ characteristics of (a) the GaN tri-gate HEMTs. (b) the etching depth of 125nm device at $V_D$=1&10.

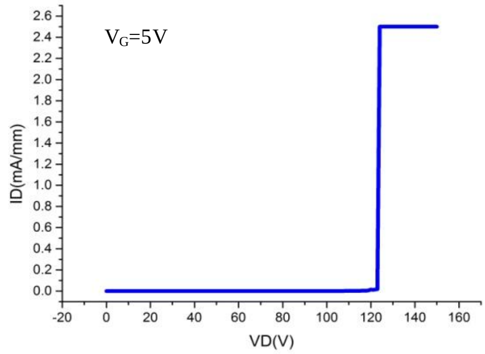


Fig.4. Breakdown voltage of the etching depth of 125nm GaN tri-gate HEMTs.

## 4. Conclusions

In this study, the GaN tri-gate HEMTs with varying body height is investigated. The GaN tri-gate HEMTs have better gate controllability as compared to the planer HEMT. The etching depth of 200nm device shows slightly lower SS with positive shift of threshold voltage. However, the etching depth of 125nm one shows much lower $R_{ON}$, higher $I_{DMAX}$ and higher breakdown voltage. The etching depth of 125nm and 200nm devices show the maximum current density of 920 mA/mm and 830 mA/mm, the maximum transconductance of 197 mS/mm and 193 mS/mm, and $I_{ON}/I_{OFF}$ ratio of $3.42\times10^{4}$ and $1.02\times10^{5}$. Both devices shows negligible drain-induced barrier lowering (DIBL).


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