

The Si-implanted Source/Drain of GaN-based High Electron Mobility Transistors by Using Stacking AlN Protection Layers

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Abstract

We presented an excellent way to improve the HEMT performance under high temperature operation. The Si-implantation into S/D for GaN-based HEMT shows a good performance at room temperature and 200°C, implies that implantation into S/D for non-alloyed Ohmic contact is work and potential.

1. Introduction

GaN-based high electron mobility transistors (HEMTs) attract lots of interests due to their high breakdown voltage and lower on-state resistance (R_{on}). For the high power applications, it is essential to improve contact resistance that the R_{on} could be diminished [1]. In general, stacking metal with thermal metallization under nitrogen atmosphere is widely served as Ohmic contact for GaN-based HEMTs, shows low specific contact resistance (ρ_s) at about $8 \times 10^{-6} \Omega \cdot \text{cm}^2$ [2]. However, the lateral alloy diffusion under thermal metallization leads to poor thermal stability under high temperature operation [3]. Hence, it is necessary to develop an advanced source/drain selective doping process with intense doping concentration that we could carry out an excellent contact resistance without thermal metallization.

Ion implantation for the selective doping is extensively used for Si-based integrated circuits (ICs) industry. However, implantation into GaN-based device has been a challenging task due to their refractory as well as GaN was grown at high temperature with high nitrogen vapor pressure. Therefore, the thermal activation of implanted dopants and damage recovery of implanted region of GaN requires annealing at temperatures above 1500°C with a nitrogen atmosphere pressure over than 15 kbar at equilibrium [4]. Some demonstrations of source/drain (S/D) implantation for non-alloyed Ohmic contacts in GaN-based HEMTs was achieved [5]. However, lower than $10^{-6} \Omega \cdot \text{cm}^2$ of the specific contact resistance is not available unless we use Si-implantation into n -type GaN [6]. In this work, we use Si-implantation into unintentionally doped GaN as S/D Ohmic contact region, and purpose to break the barrier of $10^{-6} \Omega \cdot \text{cm}^2$ for specific contact resistance. Due to we need longer thermal activation duration to activate implanted Si dopants but the crystal quality should be remained, the

stacking AlN protection layer should be employed to prevent dissociation of GaN under ultra high annealing temperature.

2. Device Modeling

The reference sample in this paper is the so-called reference HEMT without Si-implantation into S/D region. To compare with reference sample, we purpose to develop a Si-implanted S/D for GaN-based HEMT. Based on our designs, the band structure and electrical properties of the Si-implanted HEMT is calculated by APSYS simulation software, which was developed by Crosslight Software Inc.

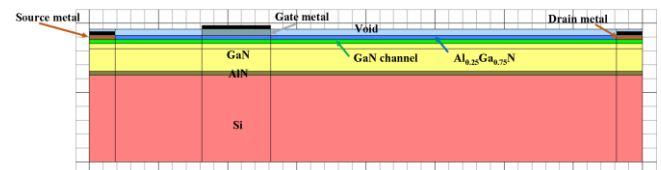


Fig. 1. Schematic diagrams of the GaN HEMTs structure for simulation.

Firstly, we simulated the band structure of metal-GaN interface. The contact between metal and semiconductor was set as an Ohmic contact, which shows the Fermi level pinning in Fig. 2 (a). Thus, the barrier height of metal-semiconductor interface shows little dependence on the work functions of semiconductor and metal. Based on our design, we decreased the work function as well as raised the doping concentration of GaN region. Hence, the Fermi level will be closed to conduction band as we increasing the doping concentration of GaN. However, we can see the Fermi level will be upper than conduction band of GaN regarding the doping concentration was reached to $1 \times 10^{19} \text{ cm}^{-3}$. Therefore, degenerate semiconductor of GaN was performed and an excess of electrons was accumulated into S/D area, that the stacking metal with thermal metallization is not necessary but we could still reach to low contact resistance in this case.

Based on our simulated results, we also simulated the I-V characteristics of HEMTs w/ and w/o S/D implantation. The $I_{DS}-V_{GS}$ curves of reference sample (w/o S/D implantation), $1 \times 10^{18} \text{ cm}^{-3}$, and $1 \times 10^{19} \text{ cm}^{-3}$ of Si doped into S/D

through ion implantation were respectively discussed. As our expected, the GaN-based HEMT with $1 \times 10^{19} \text{ cm}^{-3}$ of S/D n -doping shows a higher I_{DS} current, reached to 763 mA/mm at $V_{GS} = 2\text{V}$. The simulated I_{DS} - V_{GS} curves were plotted in Fig. 2 (b).

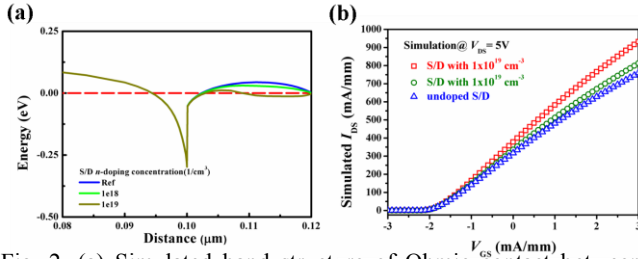


Fig. 2. (a) Simulated band structure of Ohmic contact between metal and GaN. (b) Simulated I_{DS} - V_{GS} curves for different S/D doping concentration. The device has a $2 \mu\text{m}$ gate length (L_G), a $4 \mu\text{m}$ source-to-gate distance (L_{SG}), and a $20 \mu\text{m}$ gate-to-drain distances (L_{GD}).

2. Device Fabrication

The power HEMTs device process started from the mesa isolation by inductivity coupled plasma reactive ion etching (ICP-RIE) system. Afterward, slow etching rate ICP-RIE process was employed to remove the 20-nm-thick of AlGaN barrier layer above the S/D region. The following 20-nm-thick SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) to serve as the surface protection layer under ion-implantation. To achieve $1 \times 10^{19} \text{ cm}^{-3}$ of S/D n -doping via Si implantation, we also used TRIM simulation to determine the dose of implanted Si dopants. The 30 keV with 20° tilt, 90 keV with 0° tilt, and 190 keV with 0° tilt of Si-implantation was respectively started. Afterward, SiO_2 protection layer was removed by BOE solution and further a 20-nm-thick AlN was deposited by atomic layer deposition (ALD). Following a 500-nm-thick sputtered AlN was grown on ALD-AlN as stacking AlN protection layers for 1400°C of Si dopants activation under 15 kbar NH_3 ambient. After thermal annealing, AlN layers were removed by ICP-RIE. The $\text{SiN}_x/\text{SiO}_2$ (20/280 nm) surface passivation and stacking metal system of Ti/Al/Ni/Au (20 nm/120 nm/25 nm/100 nm) was fabricated. After stacking metal deposition, a 850°C thermal annealing was carried out the ohmic contact formation for reference sample (w/o Si-implantation) but without thermal metallization for Si-implanted samples. Finally, the stacking metal system of Ni/Au (50 nm/300 nm) was served as Schottky gate metals. The device has a $2 \mu\text{m}$ gate length (L_G), a $4 \mu\text{m}$ source-to-gate distance (L_{SG}), and a $20 \mu\text{m}$ gate-to-drain distances (L_{GD}). The specific contact resistance was measured by TLM measurement, shows $7.9 \times 10^{-8} \Omega\cdot\text{cm}^2$ and $8.2 \times 10^{-6} \Omega\cdot\text{cm}^2$ for Si-implanted sample and reference sample, respectively.

3. Results and Discussion

Figure 3(a) shows the I_{DS} - V_{DS} comparison of the HEMTs between reference sample and Si-implanted S/D sample. The maximum I_{DS} of Si-implanted sample shows

805 mA/mm at $V_{GS} = 2\text{V}$, but only 729 mA/mm of I_{DS} was performed in reference sample. Derived from the results, the yielding specific on-state resistance (*spec. R_{on}*) is $1.74 \text{ m}\Omega\cdot\text{cm}^2$ of Si-implanted sample, and $2.18 \text{ m}\Omega\cdot\text{cm}^2$ of reference sample, respectively. The improved R_{on} implies that the Si-implantation into S/D with stacking AlN protection layers is an excellence solution to achieve low contact resistance without thermal metallization.

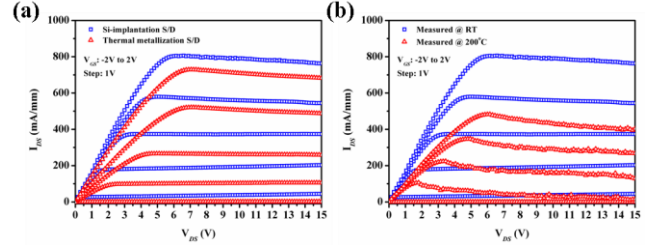


Fig. 3. (a) I_{DS} - V_{DS} curves of Si-implanted S/D HEMT and reference sample. (b) On-state I_{DS} - V_{DS} characteristics of HEMT sample with Si-implantation S/D under room temperature and 200°C , respectively.

The following thermal stability under 200°C shows good performance of Si-implanted S/D sample. The on-state resistance was increased from 1.74 to $2.96 \text{ m}\Omega\cdot\text{cm}^2$ of Si-implanted sample, but increased from 2.18 to $4.5 \text{ m}\Omega\cdot\text{cm}^2$ of thermal metallization S/D sample. The results imply that the better thermal stability was shown in non-alloyed Ohmic contact of HEMT.

This new concept and technique can trigger enthusiastic academic as well as industrial interests in various scientific areas, including crystal growth, materials, electronic devices, etc.

4. Conclusions

In this paper, we report a low contact resistance technology by using Si-implantation into S/D. Along with stacking AlN, we can avoid thermal damage under high temperature annealing, thereby low contact resistance of $7.9 \times 10^{-8} \Omega\cdot\text{cm}^2$ is achieved through 1400°C of Si dopants activation. The following thermal stability under 200°C shows good performance, implies that S/D implanted HEMT without thermal metalization is a good solution for power HEMTs.

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