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Highly Fabrication-Tolerant Shallow-Grating Coupler for Robust Coupling to Multimode "Optical Pin"

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Abstract

We present a highly fabrication-tolerant shallow-grating coupler (GC) operating at around a 1310-nm wavelength for connecting to a multimode "optical pin". We numerically show that the fabrication tolerance was improved with an optimized core thickness and was higher with an increasingly shallower grating. It was also found that a shallow GC with anti-reflection coating (ARC) layers was able to exhibit upward emitting efficiencies greater than −1 dB in a wide wavelength range of about 70 nm or even with thickness variations of the ARC layers over ±30 nm.

1. Introduction

Toward the realization of high-speed and low-power-consumption optical interconnects, we have demonstrated 25Gbps/channel error-free operation with an over 300-m multimode fiber (MMF) by using transmitter (TX) and receiver (RX) Si chips called optical I/O cores [1]. We utilized the MMF to ease the alignment difficulty of coupling a grating coupler (GC) on the TX chip to an external waveguide (WG). In addition, in order to facilitate the approach of the MMF to the GC, which was on the crowded surface of the TX chip, we introduced an "optical pin", or a vertical short multimode waveguide, between the MMF and the GC [2]. Those measures were part of our efforts to obtain the link performance at a high yield. Designing fabrication-tolerant devices as well as raising fabrication accuracies of individual optical components is also among the efforts. We, here, focus on highly fabrication-tolerant GC designs adapting to the MMF coupling via the optical pin [3, 4].

In the present work, we optimized the design of our new GCs in a silicon-on-insulator (SOI) wafer by means of analytic method and numerical simulations. We show the robustness of the upward emitting efficiency of a GC having an anti-reflection coating (ARC) against variation of etching depth of the grating, the thickness of the SOI core layer and that of the upper cladding layer.

2. Analytical and Numerical Results and Discussion

First, we investigated output stability of a plain GC structure in an SOI wafer. Figure 1 shows calculated upward emitting efficiency of the GC as a function of the etching depth of the grating and the thickness of the SOI layer at a wavelength of 1310 nm. The inset of Fig. 1 shows a schematic illustration of the cross-section of the GC we considered, which consisted of a SOI layer on a buried oxide (BOX) layer and a silicon substrate. The SOI layer had periodically arranged grooves to diffract the electromagnetic (EM) field propagating along the SOI layer and was covered with an upper cladding layer made of SiO_2. We assumed that all layers were linear, homogeneous and lossless and that the polarization of the electric field was perpendicular to the cross section. The upward emitting efficiency was defined by the equation, $\eta_{up} = P_{up} / (P_{up} + P_{down})$, where P_{up} and P_{down} were the powers of upward and downward diffracted EM fields of a 20-μm-long grating, respectively. The thickness of the BOX layer was assumed to be 2972 nm and the SiO_2 filling factor of the grating was 0.6. The period of the GC was decided such that the diffraction angle of the upward EM field in the upper cladding was about 8° with respect to the vertical direction to the Si substrate. These numerical calculations were based on the two-dimensional finite-difference time-domain (FDTD) method, and the diffraction angle was verified by Fourier transformations of the near-field pattern monitored at a plane located right above the SOI layer.

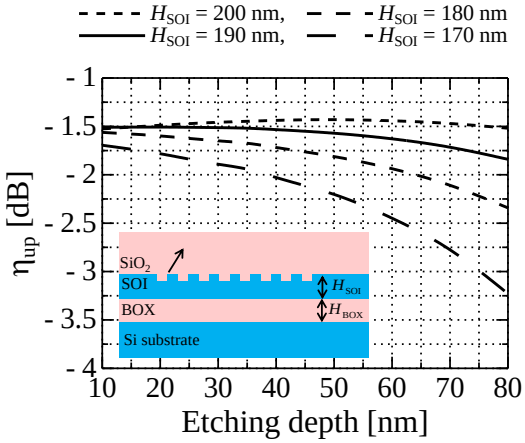

Fig. 1: Upward emitting efficiency as a function of etching depth and SOI thickness. Inset: Schematic cross-section of shallow GC. The thickness of BOX layer is H_{BOX} and that of SOI layer is H_{SOI}.

As seen in Fig. 1, the thicker the SOI layer became, the higher the upward emitting efficiency rose. When the SOI thickness H_{SOI} was 190 nm and the etching depth d was 35 nm, the upward efficiency η_{up} was −1.5 dB. In fact, this was an improvement of 1.3 dB from the performance of our

previous GC [1], which had a 170-nm thick SOI layer and a 70-nm etching depth. It is worth noting that the improved emitting efficiency was robust against the variation of the etching depth and thickness of the SOI layer. Actually, the GC required a grating longer than the previous one, since the diffraction efficiency per length of the shallow grating was small. To make such a shallow grating available as a GC, we have proposed a folded configuration of GC [4].

To further improve the upward emitting efficiency, we designed ARC layers applied to the shallow GC. The layers of the ARC were a SiO_2 layer (with a thickness H_{clad}) right on the SOI layer and a SiN layer on top (with a thickness H_{clad2}). The SiO_2 layer was inserted as a buffer to prevent scattering of light at the edge of the SiN layer area. A theoretical analysis taught us that the optimized thicknesses of the SiO_2 and SiN layers are given by the equations,

$$H_{\mathrm{clad}} = \frac{\lambda_{\mathrm{SiO2}}}{4}(2m) - \xi \qquad (1)$$

and $$H_{\mathrm{clad2}} = \frac{\lambda_{\mathrm{SiN}}}{4}(2m-1), \qquad (2)$$

where m is a positive integer, λ_{SiN} and λ_{SiO2} are wavelengths in the SiN and SiO_2 layers, respectively. ξ is an adjusting parameter; Eq. (1) shows that the effective thickness of the SiO_2 buffer layer was slightly different from half of a wavelength as the SOI layer has periodic grooves.

Figures 2 (a) and (b) show the upward emitting efficiencies as a function of (a) upper SiO_2 layer thickness and (b) SiN layer thickness at a wavelength of 1310nm. The calculations were based on the FDTD method with $H_{\mathrm{SOI}} = 190\,\mathrm{nm}$ and the etching depth $d = 35\,\mathrm{nm}$. For Fig. 2(a), the upward emitting efficiencies were calculated with the fixed $H_{\mathrm{clad2}} = 166\,\mathrm{nm}$, which was derived from Eq. (2) with $m = 1$. For Fig. 2 (b), they were calculated with the fixed $H_{\mathrm{clad}} = 440\,\mathrm{nm}$, which was derived from Eq. (1) with $m = 1$ and $\xi = d/2$. As seen in Figs. 2 (a) and (b), the thicknesses at the peaks of the efficiencies were in good agreement with those given by Eqs. (1) and (2). The range of H_{clad} to obtain the upward emitting efficiency of greater than -1 dB was about 60 nm and that of H_{clad2} was about 80 nm. These wide ranges show the robustness of the GC with respect to the variations of the layer thicknesses. As seen in Figs. 3 (a) and (b), the upward emitting efficiency of -0.9 dB was able to be reached with $H_{\mathrm{clad}} = 440\,\mathrm{nm}$ and $H_{\mathrm{clad2}} = 166\,\mathrm{nm}$.

Figures 3(a) and (b) show the upward emitting efficiency and the peak angle of the far-field pattern (FFP), respectively, as a function of a wavelength. In Fig. 3(a), we confirmed that the wavelength range for the upward emitting efficiency of greater than -1 dB was about 70-nm-wide. The optimized GC was intended to couple an optical pin. Its numerical aperture of 0.466 [2] allowed deviation angles of incidence of $\pm 17.1°$ in the core medium of the optical pin, as indicated by the two broken lines in Fig. 3(b). As seen in Fig 3(b), the peak angle of the FFP varied only within a range of about 10° and was well contained within the allowed deviation zone.

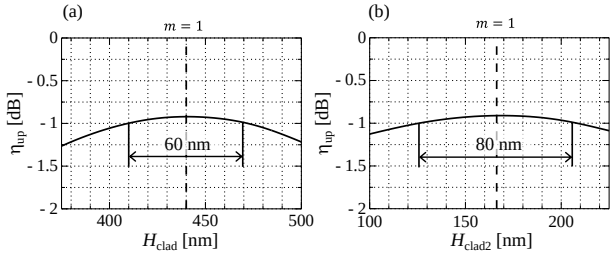

Fig. 2: Upward emitting efficiency as a function of (a) thickness of SiO2 buffer layer and (b) thickness of SiN layer.

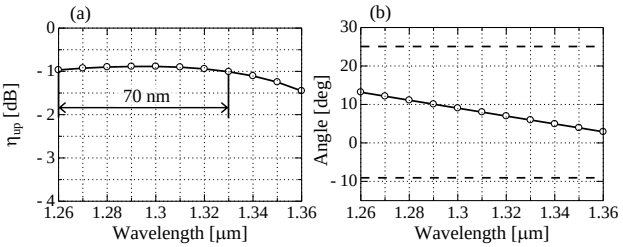

Fig. 3: (a) Upward emitting efficiency and (b) peak angle of far-field pattern as a function of a wavelength. Two broken lines indicate upper and lower limits of possible incident angles of an optical pin.

3. Conclusions

We have designed a highly fabrication-tolerant shallow-grating coupler (GC) operating at around a 1310-nm wavelength for efficiently and stably coupling to a MMF via a multimode "optical pin". The upward emitting efficiency of the GC was robust against variation of the etching depth of the grating, the thickness of core layer and those of the upper cladding layers. The wavelength range to realize the upward emitting efficiency of greater than -1 dB was as wide as about 70 nm. These results demonstrate that the shallow GC is a promising candidate to improve the optical output performance of an optical I/O chip.

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References

[1] K. Yashiki et al., "5-mW/Gbps Hybrid-Integrated Si-Photonics-Based Optical I/O Cores and Their 25-Gbps/ch Error Free Operation with over 300-m MMF", Proc. OFC, Th1G.1, Los Angeles (2015).

[2] T. Uemura et al., "125-μm-Pitch × 12-Channel "Optical Pin" Array as I/O Structure for Novel Miniaturized Optical Transceiver Chips", Proc. ECTC, Paper 5 in Session 30, San Diego (2015).

[3] D. Taillaert et al., "Grating Couplers for Coupling between Optical Fibers and Nanophotonic Waveguides", Jpn. J. Appl. Phys. 45 6071 (2006).

[4] M. Tokushima et al., "High-Efficiency Folded Shallow-Grating Coupler with Minimal Back Reflection toward Isolator-Free Optical Integration", submitted to ECOC2015.