Low-resistivity lateral PIN junction formed by Ni-InGaAsP alloy for carrier-injection InGaAsP photonic devices

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Abstract

The Ni-InGaAsP alloy was successfully fabricated at low temperature. Ni-InGaAsP alloy shows the low sheet and contact resistance as compared with implanted InGaAsP. We have successfully achieved low-resistivity lateral PIN junction with Ni-InGaAsP. The lateral PIN junction using Ni-InGaAsP also shows the large on current more than the ion implantation junction.

1. Introduction

To overcome the weak optical confinement in conventional InP photonics, we have proposed the III-V CMOS photonics platform [1-2]. By using a III-V on insulator (III-V-OI) wafer, we can obtain strong optical confinement, enabling significant reduction in device size of InP photonics. InP-based Micro bends, wavelength MUX/DEMUX, and grating coupler [3] fabricated on III-V-OI wafers are reported so far. Carrier-injection devices such as optical modulators/switches [4] and laser diodes (LDs) [5-6] have also been demonstrated on III-V-OI wafers by using lateral PIN junctions. For these carrier-injection devices, it is crucial to form low-resistivity lateral PIN junctions. We have reported the formation process of lateral PIN junctions by using Si ion implantation and Zn diffusion for reducing parasitic resistance [7]. However, the low dopant solubility in III-V materials such as InP and InGaAsP [8] leads to increase the parasitic resistance at the junction region. This parasitic resistance decrease entire injection current into PIN junctions. To solve this problem, the metal alloy with III-V materials like silicide process has been researched particularly for InGaAs and InP metal-oxide-semiconductor (MOS) transistors [9-10]. The metal alloy junction is formed at a very low temperature compared with the conventional ion implantation method. Therefore, it gives the flexibility of controlling thermal budget with keeping low resistivity in the junction. Especially, the Ni-InGaAs alloy has been reported as a quite suitable method for forming N+ S/D for MOS transistors. For photonics application, InGaAsP with a bandgap energy of more than 0.88 eV is used for the telecommunication wavelength around 1550 nm. However the formation of Ni-InGaAsP alloy has not been investigated yet. If the Ni alloy is formed in InGaAsP, we can expect to achieve a low parasitic resistance in InGaAsP PIN junctions.

In this study, we investigate the alloy between Ni and InGaAsP and apply the Ni-InGaAsP alloy for achieving lateral PIN junctions with low sheet ($R_{sheet}$) and contact resistance ($R_{contact}$).

2. Schottky junction characteristic of Ni/InGaAsP

First we investigate Schottky junction properties between Ni and InGaAsP. The 500-nm-thick p and n type InGaAsP ($\lambda_g = 1370$ nm) layers were grown by using metalorganic vapor phase epitaxy (MOVPE) on p+ and n+ InP substrate, respectively. The InP epitaxial wafers were provided by Sumitomo Chemical Co.,Ltd. Then, Ni was deposited by e-beam (EB) evaporation. Figure 1 shows the Schottky junction characteristic. The n and p type InGaAsP samples show the ohmic and Schottky behavior, respectively. It suggests that the Fermi level is pinned at the near conduction band similar to Ni/InGaAs Schottky junctions.

3. Ni-InGaAsP alloy formation

Based on above result, we tried to form the Ni-InGaAsP alloy. The 20-nm-thick Ni was deposited by EB evaporation on n and p type InGaAsP layers. Then we annealed each sample by rapid thermal annealing (RTA) for 1 min in N₂ ambient to form the Ni-InGaAsP alloy. The annealing temperature was from 250°C to 400°C with 50°C step. After RTA annealing, the unreacted Ni was selectively etched by HCl solution. Pt electrodes were formed by sputtering and lift off. Figure 2 shows the diode characteristic of Ni-InGaAsP alloy. The diode behavior was same as the native Ni and InGaAsP junction. From this result, the Ni-InGaAsP alloy is expected to be used for N+ junction of InGaAsP. To investigate of Schottky barrier height (SBH) of Ni-InGaAsP for electron, we measured the reverse bias current at the high temperature condition. The RTA temperature dependence of SBH of the Ni-InGaAsP alloy is shown in Fig. 3. The SBH of Ni-InGaAsP alloy was found to be as low as 290 mV to 320 mV regardless of the RTA temperature. This value is located between the Ni-InP and Ni-InGaAs values reported in Ref. [9] and [10]. We observed no significant degradation of junction characteristic with increasing of RTA temperature up to 400°C.
implantation owing to the low sheet resistance and contact resistance in the Ni-InGaAsP alloy.

Fig. 4 Contact resistance and resistivity of Ni-InGaAsP.

Fig. 5 Diode characteristic of PIN junction.

6. Conclusion

In this study, we investigated Ni-InGaAsP alloy for carrier-injection InGaAsP photonic devices on the III-V CMOS photonics platform. We have confirmed the formation of Ni-InGaAsP alloy which exhibiting an ohmic CMOS property for n-InGaAsP. The \( R_{\text{sheet}} \) and \( R_{\text{contact}} \) of Ni-InGaAsP were significantly lower than those of the implanted InGaAsP. Thus, we have successfully demonstrated low-resistivity lateral PIN junction by using the Ni-InGaAsP alloy and Zn diffusion, which is a quite promising fabrication process for carrier-injection InGaAsP devices with low thermal budget.

Acknowledgements

This work was supported by a Grant-in-Aid for Young Scientists (A) from MEXT. The authors would like to thank JSPS for research fellowship and Osamu Ichikawa, Hisashi Yamada, Sumitomo Chemical Company Ltd., Tsukuba, Japan, for their technical supports.

References


4. Sheet and contact resistance

For obtaining large injection current through a lateral PIN junction, low \( R_{\text{sheet}} \) and \( R_{\text{contact}} \) are necessary. Thus we evaluated the \( R_{\text{sheet}} \) and \( R_{\text{contact}} \) as a function of the RTA temperature as shown in Fig. 4. To extract the value of \( R_{\text{sheet}} \) and \( R_{\text{contact}} \), we used the transmission line method (TLM) patterns on p-InGaAsP with a carrier concentration of \( 1 \times 10^{16} \) cm\(^{-3}\). We assume that the thickness of Ni-InGaAsP (\( T_{\text{Ni-InGaAsP}} \)) was slightly increased from initial Ni thickness based on reported Ni-InGaAs case. [11] The estimated \( T_{\text{Ni-InGaAsP}} \) is 34 nm and the junction depth of Si implanted InGaAsP is 70 nm based on secondary ion mass spectrometry (SIMS) result. Each \( R_{\text{sheet}} \) of Ni-InGaAsP alloy and Si implanted InGaAsP were approximately 100\( \Omega \cdot \text{cm} \) and 450\( \Omega \cdot \text{cm} \), respectively. The converted resistivity of Ni-InGaAsP was around 350 \( \mu \Omega \cdot \text{cm} \) which is 1/8 times smaller than Si implanted InGaAsP sample. The \( R_{\text{contact}} \) of Ni-InGaAsP alloy was almost 1/100 smaller than that of the Si implanted sample. From this result, we expect to reduce the parasitic resistance of the N+ junction region.

5. PIN junction with Ni-InGaAsP alloy

To apply the Ni-InGaAsP alloy for PIN diode, we prepare a 250-nm-thick undoped InGaAsP layer on a semi-insulating (SI) InP substrate. For P+ junction, the Zn diffusion process was used by Zn-doped SOG. After spin-coating the SOG, the diffusion was carried out by RTA for 1min at 550°C. After forming the P+ region, we deposited 20-nm-thick Ni by EB evaporator. Then, the Ni-InGaAsP alloy was formed as a N+ junction by annealing at 350°C for 1 min. Finally the Pt electrode was formed on each P+ and N+ region. The fabricated PIN diode shows the fine diode characteristics as shown in Fig. 5. The ON/OFF ratio was over 10\(^3\) and the ideal factor was 1.6. The lateral PIN junction with the Ni-InGaAsP alloy shows a larger ON current than the PIN junction formed by Si ion