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A Quasi-ballistic Transport Model for Top- and Back-gated Graphene Nanoribbon Field-effect Transistors

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Abstract

A carrier transport model for graphene nanoribbon field-effect transistor (GNR FET) is obtained by using McKelvey's flux theory and quasi-ballistic transport theory. With the model, an analytical expression for drain to source current is achieved with only three fitting parameters. The model is verified with simulations, and good agreements are observed. With the model, the characteristics of drain to source current of the GNR FET with different drain biases or gate biases can be obtained very swiftly, saving much simulation time. The model will provide some design insights in the practical use of the GNR FETs.

1. Introduction

As metal-oxide-semiconductor field-effect transistor (MOSFET) scales down to the nanometer regime, silicon based channel material transistor seems to come to its performance limit. It is believed that graphene is one of the most favorable materials to be used for the channel in the near future [1-4]. With the advantages of its high mobility, excellent chemical and mechanical stability, and two-dimensional (2D) structure, graphene shows a perspective usage. However, it is well-known that large area of graphene is gapless, restricting its applications to radio frequency and analog circuits. To extend its usage to digital circuit where a band gap is needed, a large area of graphene is cut into ribbons with a width of a few nanometers. This is the so called graphene nanoribbon (GNR), where space confinement along the width direction leads to the quantization of carrier's energy, and a band gap can be achieved.

To facilitate the practical applications of GNR FETs, analytical models for drain current, subthreshold swing, transconductance, and threshold voltage are needed in circuit design and simulations. Of all, the drain current model is one of the most important.

In this paper, we use McKelvey's flux theory [5] and quasi- ballistic transport model to obtain an analytical drain current expression for GNR FETs. The analytical results match with simulations quite well, and the model is in a simplified form, including only three fitting parameters.

2. Drain current model

A GNR is a monolayer of graphene sheet patterned along a specific channel direction with a very small channel width. The cross-section view of a GNR FET is shown in Fig. 1, a layer of GNR with a channel length L, and a channel width W, is placed on a back oxide. The GNR is perpendicular to the x-direction, the channel width is along y-direction (not shown in the figure), and the channel length is along the z-direction. The biases applied to the top gate, back gate, and the drain are V_{TGS}, V_{BGS}, and V_{DS}, respectively, and the electric potential at the source is referenced to zero.

In this paper, we focus our research on semiconducting armchair GNRs, where N=3p or N=3p+1, with p being an integer, and N the total number of carbon atoms along the width direction [4,6].

The directed fluxes in a GNR can be understood from [7,8]. We define flux in this work as the carriers (electrons) passing through the channel per second, and in the unit of s^{-1}. The drain to source current, I_{DS}, is given by net charges carried by fluxes between the positive- and the negative-going fluxes,

$$I_{DS} = q\left[F^{+}(0) - F^{-}(0)\right] \qquad (1)$$

where q is the elementary charge, $F^{+}(0)$ and $F^{-}(0)$ are positive- and negative-going fluxes, respectively.

With the theories of density of states and ballistic scattering, the source- and drain-injected fluxes, $F^{+}(0)$ and $F^{-}(0)$, can be obtained, and the drain current is achieved

$$I_{DS} = \frac{qk_BT}{\pi\hbar}(1-r)\sum_m g_m \int_{x_m}^{\infty} \frac{xdx}{\sqrt{x^2 - x_m^2}} \left(\frac{1}{e^{x-\eta_F}+1} - \frac{1}{e^{x-\eta_F+U_{DS}}+1} \right) \qquad (2)$$

where r is the backscattering coefficient, it can be obtained with fitting parameters α and β [2,8]. g_m is the valley degeneracy, $x_m = E_m/k_BT$, $E_m = \pm\hbar v_F \sqrt{k_z^2 + (m\pi/W)^2}$, v_F is the Fermi velocity, k_z is the wave vector of z component, $m = \pm1, \pm2, \pm3\ldots$, $\eta_F = E_F/k_BT$, $E_F = qV_{CH}$, V_{CH} is the voltage drop across the capacitance, $U_{DS} = qV_{DS}/k_BT$, and, $\hbar$, k_B and T have their usual meanings.

3. Verification and results

To test our model, we compare our model results with those from simulations [4], and Fig. 2 presents both results. It is noticed that excellent matches are observed. The

channel length is 90 nm, the width is 4.2 nm. The thickness of the top and back gate oxide is 1 nm and 300 nm, respectively. The drain bias is 0.4 V. The low-field electron's mobility is, $\mu = 500\ \mathrm{cm}^2/\mathrm{Vs}$, and the high-field mobility can be adjusted with a fitting parameter θ [2].

Fig. 3 reveals the output characteristic of three GNR FETs with different channel lengths, L=15, 20, and 25 nm, respectively. Other structural parameters and biases are the same for all of the three transistors: W=5 nm, $t_{Tox} = 1.5$ nm, $t_{Box} = 300\,\mathrm{nm}$, $V_{T,eff} = 0.4$ V, and $V_{B,eff} = 0$ V. It is noticed that a device with a longer channel will have a smaller drain current, and the reason is that the back-scattering coefficient increases with the increase of channel length. When the drain bias is smaller than 0.4 V, the drain current increases very rapidly, after that, it increases slowly and presents a little saturation behavior.

Fig. 4 shows the output characteristic of three GNR FETs with different top-gate oxide thicknesses, $t_{Tox} = 1$, 1.5, and 2 nm, respectively. Other structural parameters and biases are: L=20 nm, W=5 nm, $t_{Box} = 300\,\mathrm{nm}$, $V_{T,eff} = 0.4$ V, and $V_{B,eff}$=0 V. A device with a thinner top-gate oxide will have a larger drain current, owing to the fact that the gate oxide capacitance is larger for a thinner oxide and more electrons are induced by the gate.

Fig. 5 demonstrates the output characteristics of the GNR FETs with different widths, W=4, 4.5, and 5 nm, respectively. All the devices are with a gate length of 20 nm, a top-gate oxide thickness of 1.5 nm, an effective top-gate bias of 0.4 V, and an effective back-gate bias of 0 V.

Fig. 6 shows the transfer characteristics of the GNR FETs with different widths. All the corresponding parameters are the same as those in Fig. 5.

Figs. 5 and 6 tell us that, a device with a larger width will have a larger drain current density (per unit width), the reason is that a larger width will have a smaller quantum effect, and the band gap will be smaller, leading to a larger drain current density.

4. Discussions

So far, a drain current model for GNR FET has been addressed and developed for the first time using McKelvey's flux theory and quasi ballistic transport theory. Source/drain series resistances are taken into account and only three fitting parameters are used. Drain current characteristics of model devices with different geometries and biases can be obtained very quickly, and the model can be used in circuit simulations.

Acknowledgments

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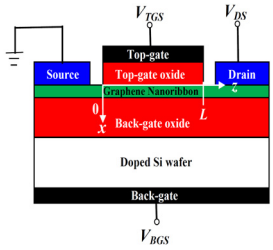

Fig. 1, Sketch map of a double-gate GNR FET.

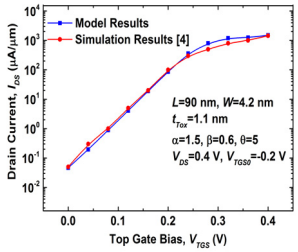

Fig. 2, Model results and simulation results of a GNR FET.

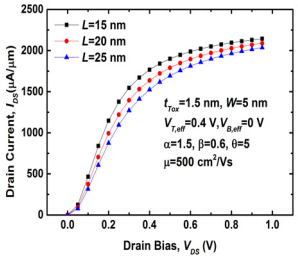

Fig. 3, Output characteristics of the GNR FETs with different channel lengths.

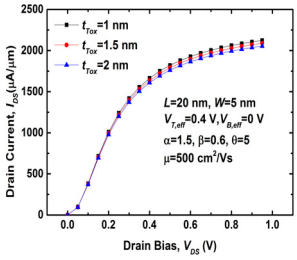

Fig. 4, Output characteristics of the GNR FETs with different top-gate oxide thicknesses.

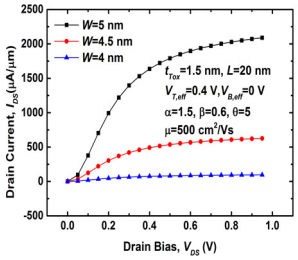

Fig. 5, Output characteristics of the GNR FETs with different channel widths.

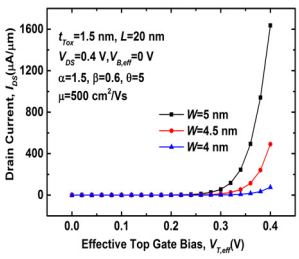

Fig. 6, Transfer characteristics of the GNR FETs with different channel widths.