Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp338-339

A Concept of Heterogeneous Circuits with Epitaxial Tunnel Layer Tunnel FETs

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***Abstract*—The epitaxial tunnel layer (ETL) TFET is an CMOS process compatible TFET. This work proposes that complementary TFET can be implemented using the same ETL material. This enables heterogeneous integration of TFET and MOSFET in current CMOS technology to leverage both the benefits of the TFET and MOSFET. By combining the characteristics of TFET and MOSFET, heterogeneous TFET-MOSFET logic gates are proposed for asynchronous datapath to enhance the energy efficiency. A 42.2–74.4% energy reduction is achieved for the 20–60ns delay range.**

1. INTRODUCTION

The tunnel FET (TFET) is an emerging device for energy-constrained applications. The steep subthreshold swing (S.S.) allows the fast transition between on-state and off-state due to the unique band to band tunneling (BTBT) mechanism. It is possible to further reduce the V_{DD} of TFET circuits without much leakage power penalty. Previous works focused on improving TFETs' device driving current but most of them are not compatible with CMOS technology [1, 2]. In our early work, a novel CMOS-compatible ETL structure using SiGe/Si hetero-material system is proposed to enhance the performance of TFET [3]. In this work, we demonstrate that this advantage allows the heterogeneous integration of MOSFET and TFET.

2. COMPLEMENTARY ETL-TFET

Fig. 1(a) illustrates the structure of the proposed ETL-TFET. Considering the fabrication feasibility, the SiGe/Si hetero-structure is applied to the ETL and to the substrate region. Ge content in the SiGe ETL is set at 80% to maintain the defect free SiGe layer [4]. Complementary fully-depleted SOI (FDSOI) MOSFETs [5] are used for performance comparison and the structures are shown in Fig. 1(b). The gate length is set to 30 nm for both TFETs and MOSFETs.

Fig.2 and 3 illustrate the on-state band diagrams of the complementary ETL-TFETs. The BTBT occurs at the overlap region between the P^+ region and the ETL for the NTFET. For the PTFET, the BTBT occurs at the overlap region between the N^+ region and the ETL. High efficient BTBT for both ETL-TFETs is achieved by applying the low band gap material in the ETL.

Fig.4 shows the transfer characteristics of ETL-TFET and MOSFET. For ultra-low power circuit design, the I_{OFF} in both TFETs and MOSFETs are target at 10pA/μm. The average S.S. (10 pA-0.1 μA) of the NTFET and the PTFET are 36mV/decade and 58mV/decade, respectively. The improved average S.S. in the NTFET is attributed to the ETL band engineering.

Fig.5 shows that the capacitance of TFET is larger than that of MOSFET because a sufficient gate-to-source overlap length is necessary to boost the BTBT current which results in a larger gate-to-source capacitance [3]. Another reason is that the on-state BTBT current of the TFET occurs at the inversion region. A strong V_{DS} dependence of gate capacitance is also observed. It will be an issue when V_{DD} scales down to ultra-low voltage region.

3. CIRCUIT PERFORMANCE

A. ETL-TFET LOGIC DESIGN

In Fig.6, a fanout-of-4 (FO4) complementary inverter is chosen to evaluate the circuit delay and transition energy. Given V_{DD} = 0.3 V, ETL-FET based inverter exhibits 16x shorter delay and 1.9x larger transition energy. The impact of the higher parasitic capacitance in the ETL-TFET causes the higher energy consumption. However, tremendous speed gain provides a chance for TFET-based circuit using lower V_{DD} and lower energy without delay penalty. To explore the advantages of the dynamic logic, an energy-delay analysis with INV/NAND/NOR combined by 50/25/25 % is performed [6]. Fig.7 shows that the TFET-based circuit creates a new operation region (orange zone) with lower energy dissipation and higher circuit performance. Dynamic circuit structure of TFET has the lowest energy dissipation compared to MOSFET-based dynamic logic and complementary logic gates realized by MOSFET or TFET.

B. TFET-BASED ASYNCHRONOUS DATAPATH

Asynchronous pipeline for an FPGA architecture is considered here to maximize the utilization of the TFET device. The asynchronous pipeline stage with precharge half-buffer (PCHB) structure consists of a gating transistor and an N-type pull-down network [9], which can be efficiently realized by NTFET-based logic and MOSFET/TFET power gating cells. A function unit used in the logic block of an asynchronous FPGA and the energy-delay curve of the AND gate pipeline stage are shown in Fig.8. The unique characteristic of NTFET expands the energy-delay space (the shaded region) for lower energy consumption. The proposed AND gate achieves 42.2 % and 74.4 % energy reductions when circuit delay is 20 ns and 60 ns, respectively. The heterogeneous TFET-MOSFET structure tailored for the

asynchronous datapath demonstrates superior performance for energy-constrained applications.

4. CONCLUSION

An ETL-TFET has been developed to enhance the S.S. and I_{ON} for both PTFET and NTFET devices. The ETL-TFET based dynamic logic consumes less energy than both FDSOI-MOSFET based complementary and dynamic logic gates. Asynchronous pipeline structure is explored to facilitate the ETL-TFET circuit design in the low-voltage applications for combating PVT variations. This provides a promising solution for future energy-efficient VLSI signal processing in the subthreshold region.

ACKNOWLEDGEMENT

This work was supported in part by the Ministry of Education, Taiwan under ATU Program and in part by the Ministry of Science and Technology, Taiwan under contract number MOST 103-2218-E-009-006.

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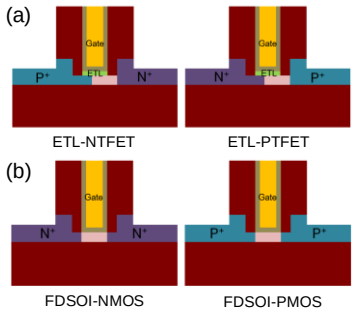

Fig.1 Schematic structure of (a) ETL-TFET and (b) FDSOI-MOSFET.

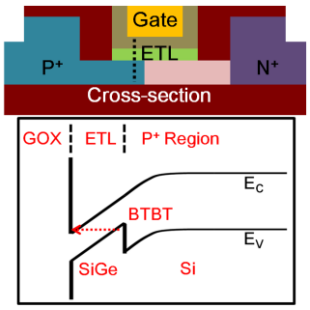

Fig.2 On-state band diagrams of ETL-NTFET in the source overlap region.

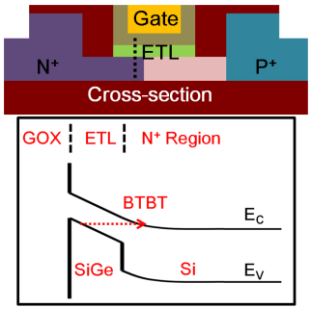

Fig.3 On-state band diagrams of ETL-PTFET in the source overlap region.

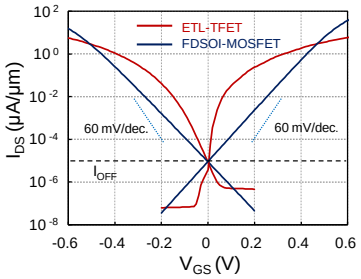

Fig.4 Transfer characteristics at V_{DS} = 0.5 V for ETL-TFET and FDSOI-MOSFET with the same I_{OFF}.

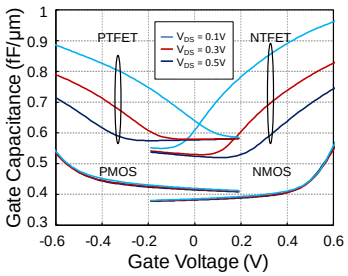

Fig.5 Gate capacitance as a function of gate voltage for ETL-TFET and FDSOI-MOSFET for different V_{DS}.

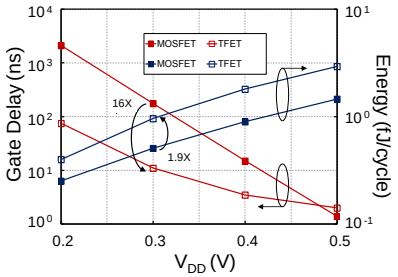

Fig.6 Delay and transition energy of FO4 inverter realized by TFET and MOSFET, respectively.

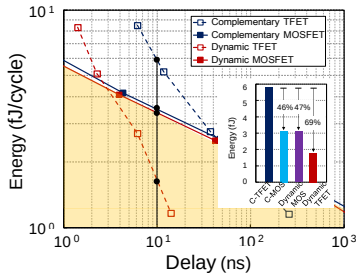

Fig.7 Energy-delay curve of complementary and dynamic logic circuit analysis with INV/NAND/NOR combined by 50/25/25%.

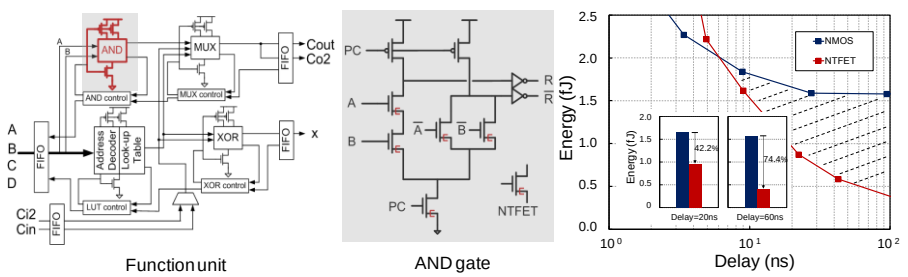

Fig.8 A function unit used in highly pipeline asynchronous FPGA datapath with proposed heterogeneous TFET-MOSFET AND gate pipeline stage.