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Gate-Stacking Engineering for Insta Ge/SiO_2/SiGe MOS Devices

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Abstract

We report a CMOS-compatible approach for generating self-aligned, gate-stacking heterostructures of Ge nano-sphere/SiO_2/$Si_{1-x}Ge_x$ (x > 0.5) shell in a single-step oxidation process. The interfacial SiO_2 layer and a $Si_{1-x}Ge_x$ shell are *in situ* formed simultaneously between the Ge nanosphere and Si substrate as a result of an exquisitely-controlled dynamic balance between fluxes of oxygen, Si and Ge interstitials. This approach provides a practically-achievable building block for Ge insta-MOS devices with size-tunable Ge gates (10–120nm), SiO_2 gate oxide (3–5 nm thick), and SiGe channels by tailoring thermal oxidation temperature, ambient, and Si substrates. High-quality interface properties for the Ge insta-MOS capaitors are evidenced by low interface-trap density of state of 4×10^{11} $cm^{-2}eV^{-1}$ and a high breakdown E-field of 8.3 MV/cm.

1. Introduction

Heterostructure of poly-Si/SiO_2/Si is one of the structural heart of metal-oxide-semiconductor (MOS) devices that culminates integrated circuit technology. Attendant to relentless reduction of feature sizes for achieving desired device performance, many high-mobility semiconductor and high-*k* dielectric materials have been proposed to replace the gate stack of poly-Si/SiO_2/Si. However, most of them are yet satisfactory for practical application because of their deficient, thermal unstable interface properties. Strained Ge into CMOS technology is one of promising approaches to boost performance of MOS transistors because of its cost effectiveness and compatibility to Si CMOS technology. However, it has been challenging for the production of high-quality Ge-on-Si MOSFETs, in particular, in situations where high-temperature thermal oxidation processes are involved. This is because of a large lattice mismatch of 4.2% existing between Ge and Si as well as the thus formed GeO_x being water-soluble and thermally-unstable.

In this paper, we demonstrated a unique, one-step insta-MOS (i-MOS) gate structure for Ge MOS devices consisting of Ge nanosphere (NP)/SiO_2/SiGe. Using the exquisitely-controlled dynamic balance between fluxes of oxygen, Si, and Ge interstitials, we are able to control thicknesses of SiO_2 and SiGe simultaneously in a single one-step oxidation process. Superior interface properties are evidenced by cross-sectional transmission electron microscopy (CTEM) and electrical properties in terms of low interface-trap density of state (D_{it}) of 4×10^{11} $cm^{-2}eV^{-1}$ and high breakdown E-field of 8.3 MV/cm.

2. Experimental

Fabrication of Ge NP/SiO_2/SiGe shell heterostructures started with a tri-layer deposition of 23-nm-thick Si_3N_4/70-nm-thick poly-$Si_{0.85}Ge_{0.15}$/5-nm-thick SiO_2 sequentially over various Si substrates including single-crystalline Si (c-Si), separation by implanted oxygen (SIMOX) Si-on-insulator (SOI), and poly-Si substrates. Poly-$Si_{0.85}Ge_{0.15}$ nano-pillars were then lithographically patterned and followed by 25min, 900°C thermal oxidation in an H_2O ambient for forming 70±5 nm Ge NP/SiO_2/SiGe shell i-MOS structures (Fig. 1). In order to tailor the depth of penetration for Ge NPs, thicknesses of the interfacial oxide layer and $Si_{1-x}Ge_x$ shell, and the Ge content within $Si_{1-x}Ge_x$ shell, an *in situ* 5 min thermal annealing was conducted at 850–900°C in an O_2 or H_2O ambient.

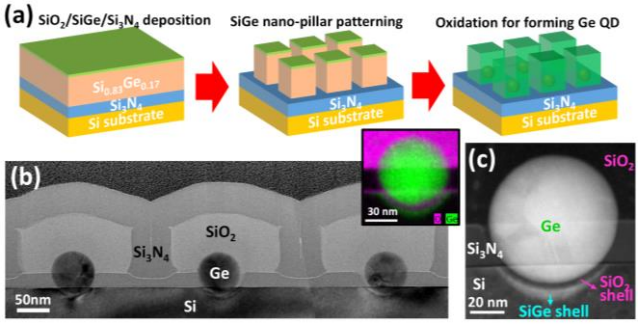

Fig. 1 I-MOS Ge NP/SiO_2/SiGe-shell heterostructure. (a) Schematic of experimental fabrication procedure. (b) CTEM and EDX mapping micrographs, (c) STEM of i-MOS structure over Si substrate.

3. Results and Discussion

Our previous reports have elaborated a cooperative mechanism between Ge, Si, and O interstitials during thermal oxidation enabling unusual Ostwald ripening and autonomous migration of the Ge nanocrystallites towards the source of Si interstitials (i.e., the underneath Si_3N_4 and Si layers). In brief, thermal oxidation of a SiGe nano-pillar converts the Si from SiGe pillars into SiO_2, squeezing released Ge atoms radially inwards to the core of oxidized pillars. Further thermal oxidation results in the consolidation via Ostwald Ripening of the growing Ge nanocrystallites and a concurrent migration of Ge nanocrystallites through SiO_2 matrix and into underlying buffer Si_3N_4 (Fig. 1). The NP size itself is lithographically controllable via control of the geometrical dimensions (width and height) of the original $Si_{1-x}Ge_x$ pillars prior to oxidation. There appears a 2.5－4nm-thick interfacial SiO_2 layer over a 3–15nm-thick $Si_{1-x}Ge_x$-shell (x = 0.5 － 0.7) with a "cup"-shape morphology that is conformal with the Ge NP and Si substrate. The thickness of the interfacial SiO_2 layer is determined by an exquisitely-controlled dynamic equilibrium that exists between the concentration of Si interstitials and external oxygen flux. Upon Ge NPs "contact" with the Si substrate, it becomes thermodynamically and kinetically favorable for Ge atoms to migrate

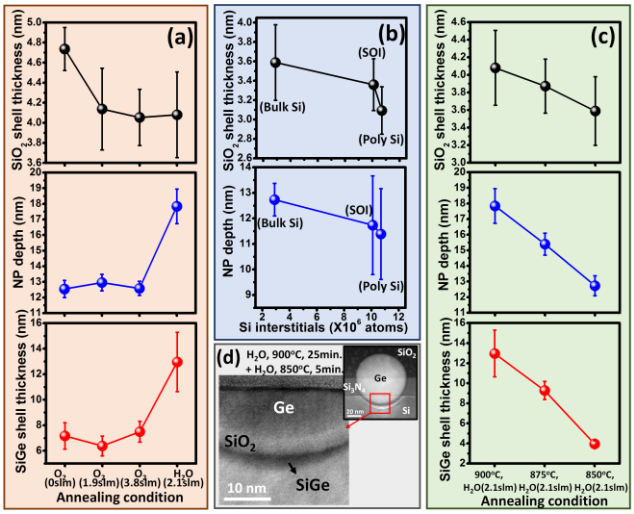

Fig. 2 Thickness of interfacial SiO_2 layer and SiGe shell as well as depth of penetration for Ge NP are tunable by flow-rates of (a) annealing gas, (b) Si interstitials flux, and (c) temperature. (d) CTEM images for 65nm Ge NPs formed by *in situ* post-oxidation annealing in an H_2O ambient at 850°C.

from the NP and dissolve within the Si substrate to form a thin, cup-shaped SiGe alloy shell that is conformal with the Si substrate and the Ge NP.

The depth of penetration for Ge NPs into Si substrate, interfacial oxide thickness, and SiGe-shell thickness appear to have a strong dependency on oxygen and Si interstitials during *in situ* postoxidation annealing. Fig. 2(a) shows that high flux of oxygen interstitials (O_2: 0－3.8slm to H_2O: 2.1sclm) is conducive for deeper penetration of Ge NPs into Si substrate (6.5－13nm) as well as for forming thinner interfacial SiO_2 layer (4.74±0.22－4.08±0.43nm) and thicker SiGe shell (12.5－18nm). This is because of catalytically enhanced location oxidation of the Si substrate that releases Si interstitials for the destruction (forming volatile SiO)/construction (SiO_2 formation) reactions surrounding the Ge NP. The fact of a reduction in interfacial oxide layer thickness ($4.74 \pm 0.22 - 4.08 \pm 0.43$nm) coupled with an enhanced SiGe shell thickness (12.5－18nm) suggests that Si interstitial flux released from the Si substrate is more conducive for the decomposition of the interfacial oxide layer than for the dynamic formation of SiO_2 ahead of the Ge NP due to the large difference in the heat formation of SiO (-426 kJ/mole) and SiO_2 (-911 kJ/mole). High flux of Si interstitials has left behind a high concentration of vacancies in Si substrate, leading to the formation of a thicker SiGe shell with a higher Ge content.

Further support for the influence of Si interstitials on the interfacial oxide layer is directly evidenced by the Ge NPs formed over substrates of c-Si, SIMOX, and poly-Si, respectively. The interfacial SiO_2 thickness reduces from 3.59±0.39, 3.36±0.27 to 3.09±0.24nm when increasing the flux of Si interstitials from 2.9×10^6 atoms released from bulk Si, 1.0×10^7 atoms from SIMOX, to 1.1×10^7 atoms from poly-Si following an 850°C, 5min H_2O annealing (Fig. 2(b)). Further downscaling the interfacial oxide layer thickness and condensation of SiGe shell is surely achievable by decreasing the annealing temperature from 900 to 850°C (Fig. 2(c)). It is constructively to note that following an 850°C, H_2O anneal heterostructures of Ge NP/3.6nm-thick SiO_2/4nm-thick SiGe possess abrupt interfaces and sharp SiGe shell with invisible defects (Fig. 2(d)), indicating superior interfacial property of our i-MOS structure that is greatly applicable for MOS device application.

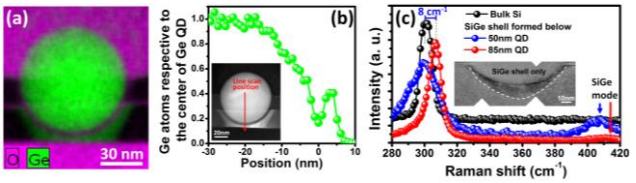

Fig. 3 (a)/(b) EDX mapping and line scan of i-MOS structure. (c) Raman spectra of SiGe shells formed right below 50 and 80nm Ge NPs and bulk Ge. The inset shows the CTEM image of a SiGe shell formed below an 85nm Ge NP that were removed by an HF dip.

EDX line scan and mapping (Fig. 3) show a large blue shift for the longitudinal optical Ge-Ge phonon line at 309cm^{-1} from the bulk value of 302cm^{-1} and a weak Raman signal at 406–414 cm^{-1}, suggesting the $Si_{1-x}Ge_x$ shell being subjected to a large compressive strain of approximately 1.6% and Ge content as high as x = 0.55–0.72 is achievable in our i-MOS structure.

Self-aligned NiGe gate/SiO_2/SiGe-channel *n*- and *p*-MOS capacitors were produced for assessment of electrical properties of our designer i-MOS structures. Invisible frequency dispersion, low D_{it} of $4-9\times10^{11}$ cm^{-2}eV^{-1}, and high breakdown *E*-field of 8.3 MV/cm were extracted from *C-V* and *I-V* characteristics (Fig. 4), confirming good gate-oxide integrity of our i-MOS system.

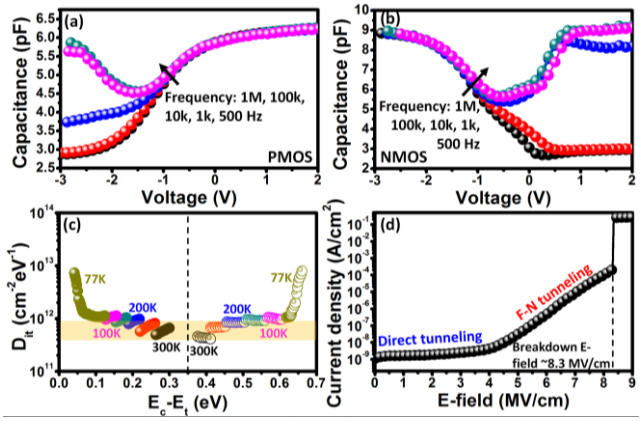

Fig. 4 (a) and (b) Frequency-dependent *C-V* characteristics of NiGe gate/SiO_2/SiGe p-MOS and n-MOS capacitors. (c) Extracted D_{it} (T = 300−77 K) and (d) *I-V* characteristic of NiGe/SiO_2/SiGe capacitors.

4. Conclusion

We have demonstrated one-step gate stack engineering for producing Ge NP/SiO_2/SiGe i-MOS structure. Compared to Ge/GeO_2/high-*k* MOSFETs, our i-MOS structure possess controllable gate-stack engineering in the gate oxide thickness and SiGe shell thickness/composition, and even strain engineering in the SiGe shell. Most importantly, superior gate oxide integrity of our i-MOS capacitors confirms of Ge NP/SiO_2/SiGe providing a practically-achievable building block for Ge-based MOS devices.

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