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Monolithic 3D (M3D) Complementary Metal-Oxide-Semiconductor (CMOS)-Nano-Electromechanical (NEM) Hybrid Circuits for Low-Power and High-Speed Reconfigurable Logic (RL) Applications

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Abstract

CMOS and nano-electromechanical (NEM) hybrid reconfigurable logic (RL) circuits are implemented by using monolithic three-dimensional (M3D) integration process. Their operation and feasibility are discussed based on simulation and experimental results.

1. Introduction

Reconfigurable logic (RL) has attracted researchers' attention thanks to its design flexibility and development time reduction. Its most well-known example is a field-programmable gate array (FPGA) as shown in Fig. 1a. The connection blocks (CBs) connect adjacent logic blocks (LBs) with each other and consist of many one-to-n or n-to-one multiplexers (MUXes). The switch boxes (SBs) connect the CBs which surround them and consist of many n-to-n MUXes. Using the CBs and SBs, the flexible data signal paths between each LB is implemented. Conventional CMOS-only RL circuits have some limitations such as low speed, high energy consumption and large chip area, because they use MOSFETs in CBs and SBs [1], [2]. In order to address these problems, CMOS-NEM hybrid RL circuits are proposed which replace MOSFETs in the CBs and SBs with NEM memory switches as shown in Fig. 1b. Their advantages are confirmed based on simulation and measurement results.

2. Simulation Results

Fig. 2a shows the structure of a NEM memory switch for RL applications. It consists of two metal line electrodes which are called Selection Line 1 (L_1) and Selection Line 2 (L_2), respectively, and a movable cantilever beam attached to the bit line (BL) which switches between L_1 and L_2. CMOS-NEM hybrid RL circuits are compared with conventional CMOS-only RL circuits in terms of performance, energy consumption and chip area by using H-SPICE and Verilog-A. For an example, the CBs are discussed in this paper. As shown in Fig. 3a, four one-to-two MUX cases have been considered for the CBs: pass gates, transmission gates, tri-state buffers and NEM memory switches. The first three cases correspond to conventional CMOS-only RL circuits. The fourth case proposed in this paper consists of one NEM memory switch and two selection MOSFETs. The operation voltage of a NEM memory switch is applied to either L_1 or L_2 through a selection MOSFET. In the case of conventional CMOS-only CBs, MOSFETs directly connect or disconnect data signal paths following control signals. However, in the case of the proposed NEM-memory-based CBs, data signal paths are maintained regardless of data signal. Thus, no control signal is necessary to maintain data signal paths in the dynamic mode and less energy is consumed. Also, because data signals are transferred through low-resistive metal lines and large contact areas rather than semiconductor channels of MOSFETs, NEM-memory-based CBs implement smaller time delay than conventional CMOS-only CBs. Figs. 3b to e show the circuit simulation results of each CB.

3. Experimental Results

In order to confirm the proposed CMOS-NEM hybrid RL circuits, the first M3D CMOS-NEM hybrid reconfigurable circuits are fabricated by using standard CMOS process. Fig. 4a shows the schematic of the fabricated 3D CMOS-NEM hybrid reconfigurable circuit. Logic and routing parts consist of CMOS and NEM memory switches, respectively. The data signals of CMOS logic gates are transferred through NEM memory switches which determine data signal paths. NEM memory switches are located in the metal layers over CMOS devices by using standard CMOS BEOL process. A NEM memory switch acts as a one-to-two multiplexer connecting two stages of CMOS inverters. Data signal paths and logic functions are determined by the beam position which varies as a function of V_{L1} and V_{L2}. Key fabrication steps are shown in Fig. 4b. First, CMOS logic circuits are fabricated on a silicon substrate by using standard CMOS FEOL process. Second, metal interconnection lines and NEM memory switches are formed by using standard CMOS BEOL process. FIB patterning has been used only to define small air gap patterns and can be easily replaced by conventional optical photolithography for mass production. Finally, the intermetal dielectric (IMD) layers surrounding NEM memory switches are selectively removed to release the beam by using hydrofluoric acid (HF) vapor etch.

Fig. 5 shows the SEM images of the fabricated 3D CMOS-NEM hybrid reconfigurable circuit. The output of the first CMOS inverter is transferred to the beam of a NEM memory switch through vias. In this work, the L_1 of the NEM memory switch is connected to Out 1 node while L_2 is connected to the input of the second CMOS inverter through vias. It means that the output of the first inverter is transferred to either Out 1 node or the input of the second inverter depending on the beam position of the NEM memory switch.

Fig. 6a shows the measurement results of State 1. V_{in} is transferred to V_{out1} through the first inverter and the NEM memory switch, which leads to "V_{in}=/V_{out1}" logic function. Subsequently, the state of the NEM memory switch is converted from State 1 into State 2 and then the same procedure is repeated except that V_{L2} ramps up this time rather than V_{L1}. In this case, the logic function becomes "V_{in}=V_{out2}". Fig. 6b shows the measurement results of State 2 when V_{in} is transferred to V_{out2} through two stages inverters and one NEM memory switch.

4. Summary

M3D CMOS-NEM hybrid RL circuits have been proposed, simulated and implemented. NEM memory routing switches are vertically integrated over CMOS logic circuits by using

standard CMOS process. The proposed NEM-memory-based RL circuits feature higher speed, lower energy consumption and smaller chip area than conventional CMOS-only RL circuits.

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References

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[2] K. Compton *et al.*, *ACM Computing Surveys*, vol. 34, no. 2, pp. 171-210, June 2002.

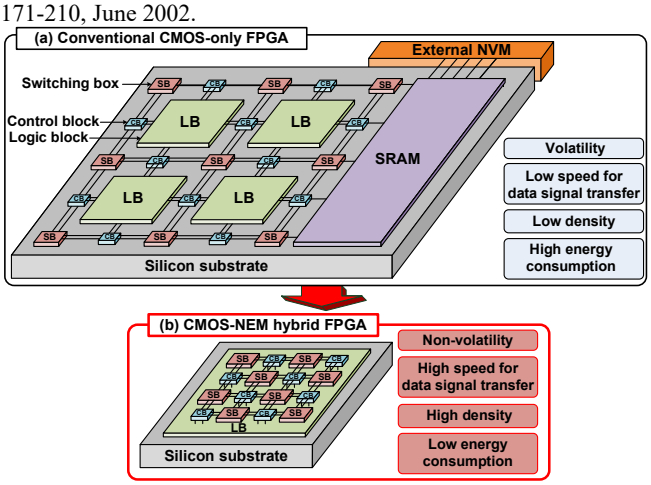

Fig. 1. Block diagrams of (a) conventional CMOS-only FPGA and (b) the proposed CMOS-NEM hybrid FPGA.

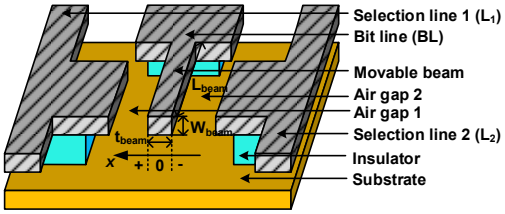

Fig. 2. Proposed NEM memory switch.

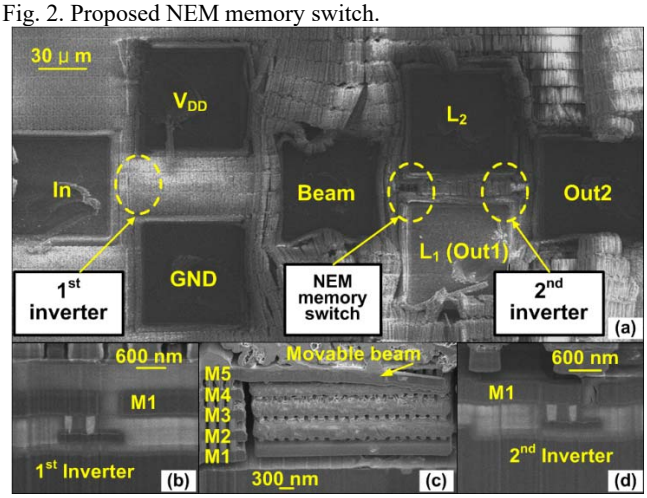

Fig. 5. (a) Plan view of the fabricated M3D CMOS-NEM hybrid reconfigurable circuit. The circuit schematic is shown in Fig. 4a. The cross-sectional view of (b) the first inverter, (c) the NEM memory switch and (d) the second inverter.

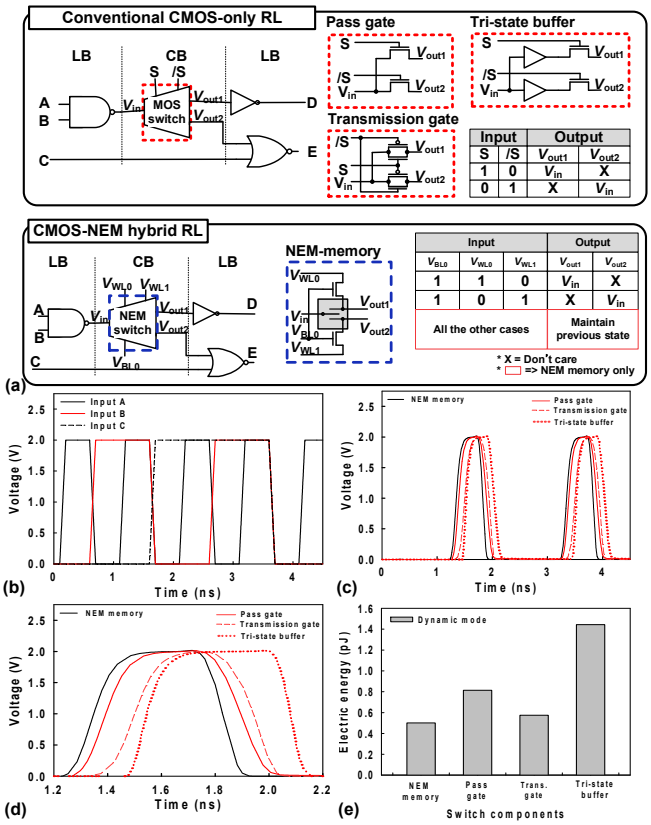

Fig. 3. (a) CBs of pass gates, transmission gates, tri-state buffers and NEM memory switches. (b) Input data signals of the CBs. (c) Output data signal *D* of the CBs. (d) Enlarged output data signal *D* shown in (c). (e) Energy consumption of various CBs per cycle.

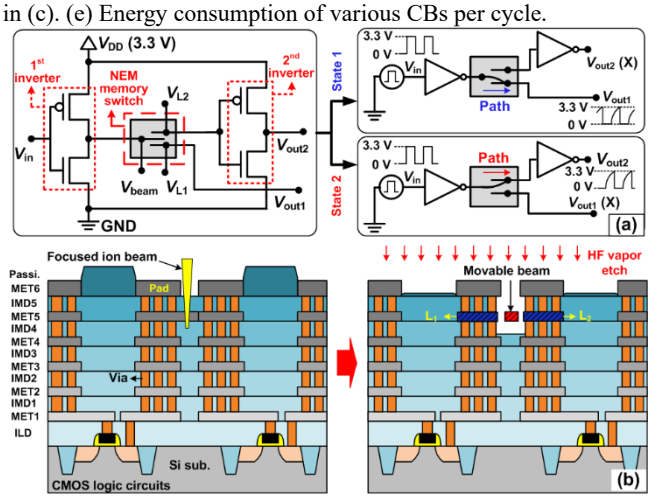

Fig. 4. (a) Schematic and (b) key fabrication process of the M3D CMOS-NEM hybrid RL circuit.

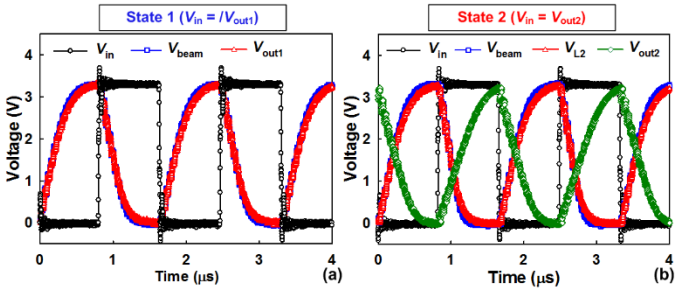

Fig. 6. Data signal transfer of the fabricated M3D CMOS-NEM hybrid reconfigurable circuit (a) in State 1 and (b) in State 2.