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Stackable MoS_2 FinFETs Using Solid CVD Developed Through Fully CMOS-Compatible Process Technology

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Abstract

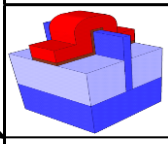
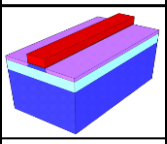
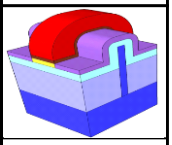
Stackable 4 nm ultra-thin body (UTB) FinFETs using chemical vapor deposition (CVD) deposited molybdenum disulfide (MoS_2) channels were developed through fully complementary metal oxide semiconductor compatible process technology. Adding several molecular layers (approximately 7 X) of the transition metal dichalogenide (TMD) MoS_2 on the back-gate Si fin resulted in improved μ_n of the Si-based FinFETs. The MoS_2 UTB FinFETs also represent a means of providing FinFETs with a new feature, namely strong back-bias control of threshold voltage (V_{th}). The novel TMD channels produced through the solid CVD method were a promising technology for low-power and scaled FinFETs in 2D and 3D ICs.

1. Introduction

3DFETs can improve sub-20 nm complementary metal-oxide semiconductor (CMOS) node performance and substantially reduce supply voltage and short channel effects [1]. However, the traditional silicon channel must be replaced by high mobility materials in future VLSI applications [2,3]. Heterogeneous 2D atomic crystals such as transition metal dichalcogenide (TMD) have atomically smooth surfaces without dangling bounds and favorable mobility in chemical vapor deposition (CVD) deposited films of atomic-scale thickness. They are attractive enablers of ultimately scaled transistors and 3D ICs [1,4]. However, a manufacturing flow must be realized using low temperature semiconductor processes [5] and TMD through CVD [6]. This paper presents a CMOS process compatible TMD 3D transistor technology using novel molybdenum disulfide (MoS_2) channel FinFETs with improved electron mobility (μ_n) of the N devices.

Channel materials such as Si, Ge, and III-V typically face process, mobility, or quantum capacitance challenges at ultra-thin body (UTB) thicknesses [3]. Advanced 2D TMD is an ideal channel material for its unique sub-nm monolayer UTB [7] potential and effective transport property at nm thinness [4]. CVD of TMD is compatible with CMOS process integration [6] and suitable for UTB formation [8]. This paper presents a 4 nm thin MoS_2 body FinFETs that has dynamically adjustable threshold voltage (V_{th}) with back-bias control [9] for low-power CMOS technology applications [10]. In comparison to previously published advanced transistors, this work reports the largest width and footprint, excellent back gate control, and high scaling ability in low-nm VLSI technology [11,12] (Table 1).

TABLE I
COMPARISON OF BULK FINFETS, UTBSOI/ FDSOI AND TMD FINFETS.

	Bulk FinFET	UTBSOI/ FDSOI	TMD FinFET
			
body formation	etching	bonding	CVD
W/footprint ratio	large	regular	large
back gate control	poor	good	excellect
scaling ability (node)	very good (> 5 nm)	good (> 10 nm)	excellent (> 2 nm)

2. Results and Discussions

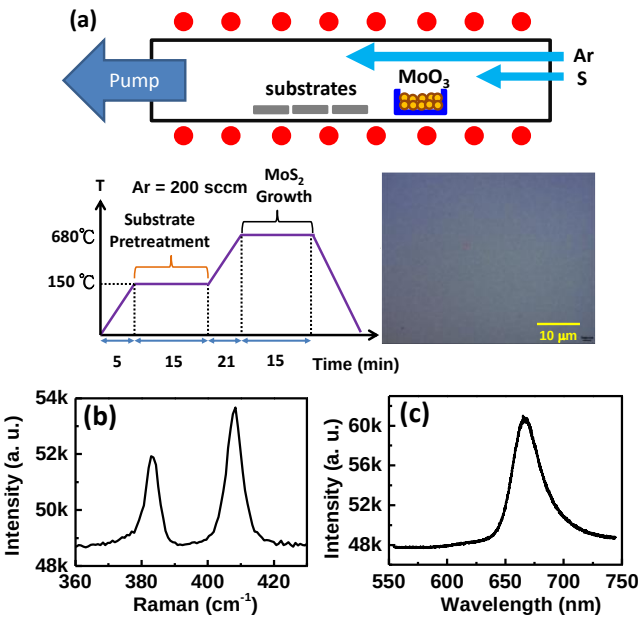


Fig. 1 (a) Growth of MoS_2 film by CVD. Photo image of uniform few-layer MoS2 film on oxide coated wafer (b) Raman and (c) PL spectra of the CVD few-layer MoS_2 film.

This study applied previously published low temperature 3DFETs technology [13]. A minimal-layer MoS_2 growth step was inserted after blocking oxide deposition and cleaning. Minimal-layer MoS_2 was successfully integrated into 3DFETs technology through low-temperature CVD and optimum treatment with the number of MoS_2 layers.

A. MoS_2 Growth by CVD

The MoS_2 CVD process is illustrated in Fig. 1(a). High-quality monolayer MoS_2 films can be grown on a blocking oxide-coated flat wafer surface. In Figs. 2(b) and (c), Raman and photoluminescence spectra confirm the high quality of the few-layer MoS_2 films grown by the advanced CVD. In Fig. 2, the TEM image shows the 6-layer (4 nm) MoS_2 body channels grown over the back-gate Si fin surface with perfect continuous coverage. After high-k metal gate deposition, a 30 nm long front gate is formed using our nano injection lithography (NIL) technique [8].

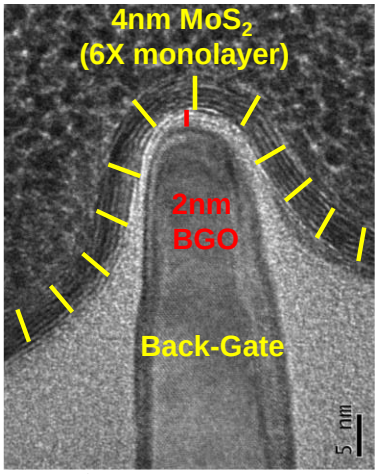


Fig. 2. The TEM image of MoS_2 body on MoS_2 FinFETs with Si back gate. Front gate HKMG is to be deposited.

B. MoS_2 FinFETs Characteristics

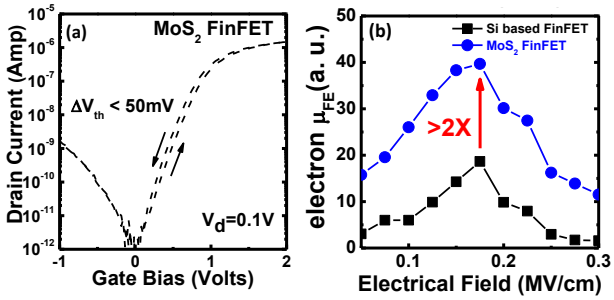


Fig. 3 (a) Gate bias sweeping and (b) calculated field-effect nobilities for the MoS_2 FinFETs.

Fig. 3 shows the transfer and output characteristics of MoS_2 FinFETs with a 30 nm gate length and 6-layer (4 nm) MoS_2 body. The front-gate MoS_2 FinFETs device has an on/off ratio larger than 10^6 and I_{on} of approximately 200 μA/μm for 0.1 volt operation bias. The 4 nm MoS_2 FinFETs can operate with back-gate bias alone in 2 nm thin BGO (Fig. 4); however, the main purpose of the back gate is to adjust the front V_{th} of the MoS_2 FinFETs as shown in Fig. 4. A back-gate bias can thus correct device variations or dynamically configure a device as a high-performance or low energy consumption device to achieve higher speed and lower power applications. The 2 nm thin BGO greatly enhances the V_{th} sensitivity to back-gate bias in comparison to a thick BGO. The 4 nm thin body and back-gate control MoS_2 FinFETs yields a record high I_{on} performance in MoS_2 devices [14,15].

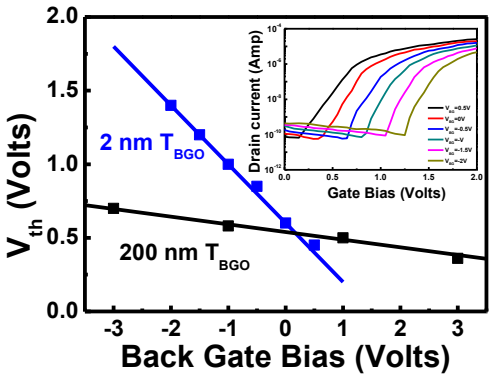


Fig. 4. Thin back-gate oxide enhances V_{th} sensitivity to back-gate bias. Inset shows back-gate bias control with TBGO (2 nm).

3. Conclusions

In this study, a 4 nm MoS_2 UTB FinFETs with back-gate control is proposed and demonstrated for the first time. The MoS_2 FinFETs channel was deposited using a CVD fully CMOS-compatible process. The μ_n of the MoS_2 FinFETs is improved by more than 2 times compared with Si-based FinFETs. The 2 nm thin back-gate oxide enables 0.5 V of V_{th} shift with a 1.2 V change in back bias of the MoS_2 UTB FinFETs. This stackable MoS_2 FinFETs using solid CVD can be fully integrated in current VLSI process technology.

Acknowledgments

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References

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