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A New Scale-Length Model for Short-Channel Monolayer and Bilayer Transition Metal Dichalcogenide (TMD) Field-Effect Transistors

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Abstract

In this work, we present a scale-length model for short-channel monolayer and bilayer transition metal dichalcogenide (TMD) field-effect transistors. The new expressions of the scale length for both ultra-thin-body (UTB) and double-gate (DG) TMD FETs are derived by considering the impact of fringe fields from the high-K gate dielectric. Our model has been verified with 2D numerical simulations for TMD devices with gate length down to 5.9 nm based on ITRS 2028 low-power technology node. Our new scale-length model can be employed by a surface-potential based model to enable a compact model for short-channel TMD devices.

1. Introduction

Because of their atomic-scale thickness, pristine surfaces and adequate bandgap energies, 2D semiconducting transition metal dichalcogenides (TMDs) such as MoS_2 and WSe_2 have garnered substantial interest as potential channel materials for future ultimately scaled low-power CMOS devices [1]–[4]. To enable circuit explorations using the ultra-scaled TMD devices, an adequate compact model is indispensible. Although several compact *I-V* models for TMD FETs have been provided [3]–[4], a short channel TMD FET model is still lacking. In [4], the model in subthreshold regime can only work for TMD devices with channel length larger than 30 nm due to short-channel effects. It was also pointed out [4] that, for 2D TMD FETs with so thin a channel, the lateral field through the gate dielectric demands careful consideration.

In this work, by incorporating the impact of lateral fields through the gate dielectric, we develop a new scale-length model for short-channel UTB and DG TMD FETs.

2. Methodology

Fig. 1(a) shows the schematic of a TMD FET in this study. Pertinent parameters of monolayer and bilayer MoS2 are listed in Table. I. Fig. 2 outlines the methodology of our scale-length model derivation for short-channel TMD FETs. The new expressions of scale length (Eqn. (4) and Eqn. (5)) and channel potential (Eqn. (3)) are obtained by applying Gauss's law to both the gate dielectric (Eqn. (2)) and channel (Eqn. (1)) regions as shown in Fig. 1(b). Based on the potential solution, the subthreshold drain current can be derived [5]. Our model shows a fairly good agreement with the numerical simulation [6] which carried out with a constant-mobility drift-diffusion model.

3. Results and Discussion

Fig. 3 shows that, albeit our model and the model in [4] yield the same results as the numerical ones for long-channel UTB devices (L = 50 nm), their short-channel behaviors are quite different. It can be seen that our model shows a fairly good agreement with the numerical results for the device with L = 5.9 nm based on ITRS 2028 low power (LP) technology node [7], while significant discrepancy exists between the model in [4] and numerical simulation. Fig. 4 compares the subthreshold swing (*SS*) of UTB device versus channel length (L) characteristics extracted from both models and numerical simulation. This demonstrates that our model possesses a fairly good scalability in channel length. Fig. 5 compares the output resistances of TMD FETs in the subthreshold regime for both models with numerical simulation. Fig. 6 shows that, for a given EOT, the electrostatic integrity of the short-channel UTB TMD FET degrades significantly with increasing gate dielectric constant (i.e., physical dielectric thickness). It also shows that our model agrees well with the numerical results.

Fig. 7 shows that, our new scale-length model can be utilized not only for UTB devices (Eqn. (4)) but also for DG devices (Eqn. (5)). To capture this short-channel behavior, the dependence on the gate dielectric constant of the scale length has to be accurately modeled, as shown in Fig. 8. Note that the dependence on the gate dielectric constant of the scale length for DG devices is slightly weaker than that for UTB devices due to the superior gate control of the DG structure.

Besides, our new scale-length model can be employed by BSIM-IMG threshold-voltage shift model [8] to enable compact modeling, as shown in Fig. 9. The drain current increases with increasing gate dielectric constant due to the drain-induced barrier lowering (DIBL). Fig. 10 shows that our new model can also be used for bilayer TMD FETs.

Acknowledgements

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References

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[5] X. Liang *et al., IEEE TED,* Sep. 2004.
[6] *ATLAS User's Manual*, SILVACO
[7] ITRS (http://www.itrs.net/)
[8] *BSIM-IMG 102.6.0 Technical Manual*.

Table I. Pertinent parameters [1], [2] of monolayer and bilayer MoS_2 used in this work.

Parameter	Monolayer MoS_2	Bilayer MoS_2
Band-gap [eV]	1.67	1.544
Electron affinity [eV]	4.28	4.29
Dielectric constant	4.8	6.9
Effective mass [m_0]	m_e = 0.467	m_e = 0.462

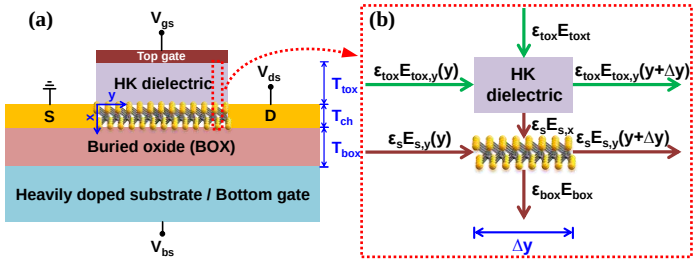

Fig. 1. (a) Schematic of a monolayer TMD FET with an atomic-scale thickness (T_{ch} ~ 0.65 nm). $T_{tox/box}$ are physical gate dielectric and BOX thickness, respectively. (b) Zoomed-in-view of an infinitely-thin (Δy) Gaussian box composed of the gate dielectric and the channel region. The arrows represent the directions of electric flux within the gate dielectric and the channel. $\varepsilon_{s/tox/box}$ are dieletric constants of the channel, gate dielectric and BOX, respectively.

Gaussian enclosure inside the channel region:

$$qN_{ch}\Delta y = T_{ch}[\varepsilon_s E_{s,y}(y+\Delta y) - \varepsilon_s E_{s,y}(y)] + \Delta y[\varepsilon_{box}E_{box} - \varepsilon_s E_{s,x}] \quad (1)$$

Gaussian enclosure inside the gate dielectric region:

$$E_{s,x} = \frac{\varepsilon_{tox}}{\varepsilon_s}\frac{[\phi_s(y) - V_{gs} + V_{fb}]}{T_{tox}} - \frac{\varepsilon_{tox}}{\varepsilon_s}\gamma EOT\frac{dE_{tox,y}(y)}{dy} = \frac{\varepsilon_{tox}}{\varepsilon_s}\frac{[\phi_s(y) - V_{gs} + V_{fb}]}{T_{tox}} - \frac{\varepsilon_{tox}}{\varepsilon_s}\frac{EOT}{\eta}\frac{dE_{s,y}(y)}{dy} \quad (2)$$

where $E_{s,y}(y) = \gamma \cdot \eta \cdot E_{tox,y}(y)$, $\gamma = \varepsilon_{tox}/\varepsilon_{SiO_2}$

The channel electrostatic potential solution:

$$\phi_s(y) = \phi_{s,long} + (V_{bi} - \phi_{s,long})\frac{\sinh[(L-y)/l]}{\sinh(L/l)} + (V_{bi} + V_{ds} - \phi_{s,long})\frac{\sinh(y/l)}{\sinh(L/l)} \quad (3)$$

where

$$\phi_{s,long} = \frac{-qN_{ch}T_{tox}T_{box} + \varepsilon_{tox}T_{box}(V_{gs} - V_{fb}) + \varepsilon_{box}T_{tox}(V_{bs} - V_{fbb})}{\varepsilon_{tox}T_{box} + \varepsilon_{box}T_{tox}}$$

New characteristic length expression for UTB structures:

$$l = \left[\frac{\varepsilon_s T_{ch}T_{tox}T_{box}}{\varepsilon_{tox}T_{box} + \varepsilon_{box}T_{tox}} + \frac{1}{\eta}\frac{\varepsilon_{tox}^2}{\varepsilon_{SiO_2}}\frac{EOT^2 T_{box}}{\varepsilon_{tox}T_{box} + \varepsilon_{box}T_{tox}}\right]^{\frac{1}{2}} \quad (4)$$

New characteristic length expression for DG structures:

$$l = \left[\frac{\varepsilon_s T_{ch}T_{tox}T_{box}}{\varepsilon_{tox}T_{box} + \varepsilon_{box}T_{tox}} + \frac{2}{\eta}\frac{\varepsilon_{tox}^2}{\varepsilon_{SiO_2}}\frac{EOT^2 T_{box}}{\varepsilon_{tox}T_{box} + \varepsilon_{box}T_{tox}}\right]^{\frac{1}{2}} \quad (5)$$

Fig. 2. The methodology of our scale-length model derivation for short-channel TMD FETs. E_{box} is the vertical field on the top of BOX and N_{ch} is the channel doping. $E_{s,x}$ and $E_{s,y}$ represent the vertical and lateral components of channel electric fields, respectively. $E_{tox,y}(y)$ is the average lateral electric field within the gate dielectric. $V_{fb/fbb}$ are the front/back-gate flat-band voltages. ϕ_s is the channel potential. η is a model parameter.

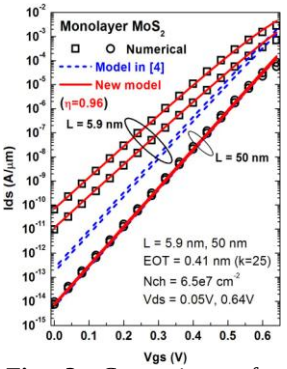

Fig. 3. Comparison of our model and the model in [4] for UTB TMD FETs.

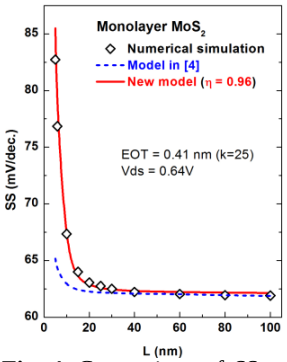

Fig. 4. Comparison of *SS* versus *L* characteristics for our model, the model in [4].

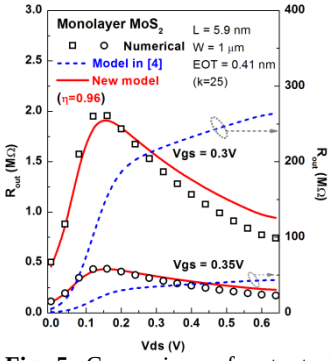

Fig. 5. Comparison of output resistances for our model, the model in [4], and numerical simulation.

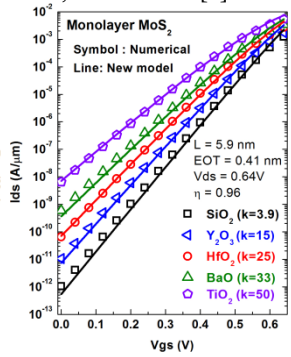

Fig. 6. Comparison of our model and numerical simulation for UTB TMD FETs with various gate dielectrics.

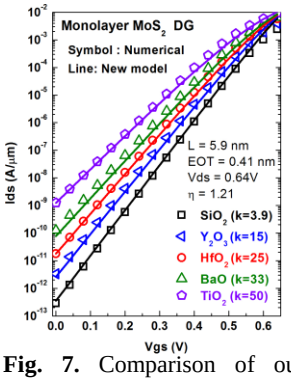

Fig. 7. Comparison of our model and numerical simulation for DG TMD FETs with various gate dielectrics.

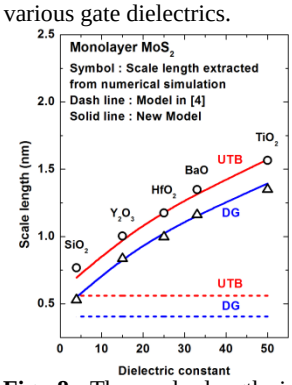

Fig. 8. The scale length increases with the gate dielectric constant for both UTB and DG devices.

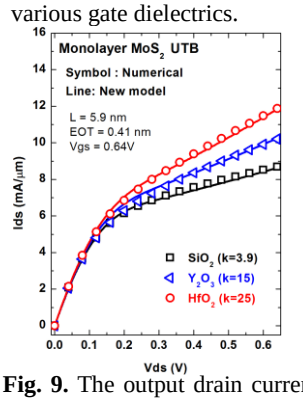

Fig. 9. The output drain current under strong inversion increases with the gate dielectric constant.

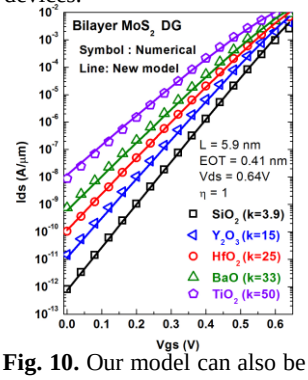

Fig. 10. Our model can also be used for bilayer TMD FETs with various gate dielectrics.