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Impacts of Device Design and Variability on 6T/8T SRAM Cells with MoS_2-n/WSe_2-p MOSFETs for 5.9nm node

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Abstract

We investigate the impacts of device design and variability on the cell stability of MoS_2-n/WSe_2-p 6T/8T SRAM cells in super-threshold and near-threshold regimes for ITRS 2028 (5.9nm) node. Our study indicates that, with superior device electrostatics, the monolayer MoS_2-n/WSe_2-p SRAM exhibits better stability than the bilayer counterpart. With source/drain underlap design, the read static noise margin (RSNM) of bilayer SRAM can be improved and becomes comparable to the monolayer SRAM. Moreover, due to severe work function variation, the monolayer/bilayer MoS_2-n/WSe_2-p 6T SRAMs operating in near-threshold regime may fail to meet the 6σ RSNM yield requirement. The RSNM variation can be mitigated using the standard 8T SRAM cell to meet the 6σ RSNM yield requirement.

1. Introduction

Due to their atomic-scale thickness and adequate band-gap, 2-D transition metal dichalcogenides (TMDs) devices such as MoS_2 and WSe_2 MOSFETs [1-4] are very attractive for future extremely-dense SRAM arrays (Fig. 1). For the extremely scaled transistors targeting the ITRS 2028 5.9nm node [5], the impact of random variations such as metal-gate work function variation (WFV) [6, 7] on the SRAM array can be crucial, particularly for ultra-low power near-/sub-threshold IoT applications. Compared with monolayer TMD devices, bilayer TMD devices have been shown to exhibit higher mobility at the expense of electrostatic integrity (EI) [2-4]. In our previous study [8], we have evaluated and benchmarked the performance of monolayer and bilayer TMD based 6T SRAM cells for super-threshold operation.

In this work, we investigate the cell stability of MoS_2-n/WSe_2-p 6T/8T SRAM cells in super-threshold and near-threshold regimes based on ITRS 2028 (5.9nm) node, with particular emphases on the trade-off between EI (monolayer favored) and carrier mobility (bilayer favored), and the impacts of the source/drain underalp design and the metal-gate WFV.

2. Device Design and TCAD Simulation Methodology

In this work, monolayer and bilayer MoS_2-n/WSe_2-p devices are designed with equal I_{off} = 5nA/μm and 10pA/μm at V_{DD}=0.64V and 0.4V, respectively (Fig. 2), and pertinent device parameters based on ITRS 2028 node (Table I). The source-to-drain direct tunneling is assumed to be negligible due to the relatively large effective masses of TMDs [2, 3]. To investigate the cell stability of MoS_2-n/WSe_2-p SRAMs, TCAD mixed-mode simulations [9] are performed with judiciously chosen physical properties of MoS_2/WSe_2 (listed in Table II). The carrier transport model is carefully calibrated with the dissipative quantum transport model using NEGF formalism in [3]. To assess the WFV, the Voronoi TCAD atomistic simulation methodology [12] is carried out with the grain size = 4.3nm [6] and 2nm [7], respectively.

3. MoS_2-n/WSe_2-p Super-threshold SRAMs at V_{DD}=0.64V

Fig. 3 compares the nominal read and write static noise margin (RSNM and WSNM) for monolayer and bilayer super-threshold 6T SRAM cells at V_{DD}=0.64V. The results show that, albeit the larger $V_{READ,0}$ (read disturb) of monolayer SRAM, its RSNM is still larger than the bilayer counterpart due to the better EI of monolayer TMD devices (and thus the steeper transition of butterfly curve shown in Fig. 3(a) inset). Compared with the WSNM (Fig. 3(b)), the RSNM is the limitation of cell stability.

Gate-to-source/drain underlap design may be used for better immunity to short-channel effects, and its impacts on the stability are investigated in Fig. 4. Fig. 4(a) shows that, with source/drain underlap design (e.g., $L_{underlap}$=2nm), the RSNM of bilayer SRAM improves and becomes slightly larger than the monolayer SRAM counterpart due to the improved subthreshold swing.

4. MoS_2-n/WSe_2-p Near-threshold SRAMs at V_{DD}=0.4V

The cell stability of monolayer and bilayer SRAMs at V_{DD}=0.4V (near-threshold) is assessed in Fig. 5. The results show that the monolayer SRAM exhibits larger RSNM and smaller WSNM than the bilayer counterparts. Besides, the disparity of RSNM between monolayer and bilayer SRAMs at V_{DD}=0.4V (Fig. 5(a)) is larger than that at V_{DD}=0.64V (Fig. 3(a)) due to the increasing relevance of EI to stability under near-threshold operation. Similar to the super-threshold case (Fig. 4), the underlap design improves the RSNM of bilayer SRAM under near-threshold operation, as shown in Fig. 6(a).

Fig. 7 assesses the impacts of WFV on the RSNM variability of 6T MoS_2-n/WSe_2-p near-threshold SRAM cells. In Fig. 7(a), with grain size = 4.3nm, the RSNM μ/σ ratios of both monolayer and bilayer 6T SRAMs fail to meet the 6σ requirement (i.e., $\mu/\sigma \geq 6$). Fig. 7(b) indicates that, even with a smaller grain size (=2nm), the monolayer and bilayer 6T SRAMs still fail to achieve the 6σ requirement. To achieve adequate μ/σ ratio, the standard 8T SRAM cell [13] may be used, and its RSNM variability is evaluated in Fig. 8. It can be seen in Fig. 8(a) that both the monolayer and bilayer 8T SRAMs offer satisfactory RSNM μ/σ ratios (i.e. > 6). With grain size reduced to 2nm (Fig. 8(b)), the RSNM μ/σ ratios of monolayer and bilayer 8T SRAMs further increase, as expected. In other words, using the 8T cell structure, the impacts of WFV on RSNM may be mitigated. Also notice that the bilayer SRAM outperforms the monolayer one due to its superior WSNM.

The source/drain contact resistance (R_{SD}) has been a critical issue for TMD devices [4], and its impacts on SRAM stability are shown in Fig. 9. Fig. 9(a) reveals that, at V_{DD}=0.64V (super-threshold operation), the RSNM and WSNMs for both the monolayer and bilayer SRAMs decrease with increasing R_{SD}, while they remain nearly unchanged at V_{DD}=0.4V (near-threshold operation) shown in Fig. 9(b). Namely, the high R_{SD} of TMD devices may be less of an issue for low-voltage TMD-based SRAMs for IoT applications.

Acknowledgement

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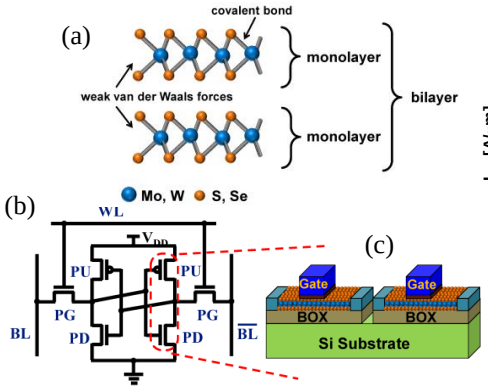

Fig. 1. (a) Schematic atomic structure of MoS_2/WSe_2. The thickness of monolayer TMD is ~0.7nm. (b) Circuit schematic of a 6T SRAM cell. (c) SRAM cell composed of extremely scaled MoS_2-n/WSe_2-p devices.

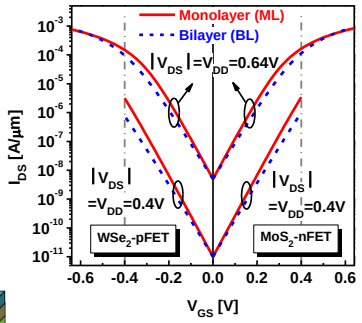

Fig. 2. I_{DS}-V_{GS} characteristics of MoS_2-n and WSe_2-p devices with equal I_{off}=5nA/μm and 10pA/μm at V_{DS} = V_{DD} = 0.64V and 0.4V, respectively. The mobility of bilayer TMDs is assumed to be 1.6X of that for monolayer TMDs based on the experimental data in [4].

Table I. Pertinent device parameters used in this work based on ITRS 2028 (5.9nm) technology node.

ITRS 2028 (5.9nm) technology node		
L_g	EOT	T_{BOX}
5.9nm	0.41nm	10nm

Table II. Material parameters for monolayer/bilayer MoS_2 and WSe_2 used in this work [1, 10, 11]. m_e and m_h denote the electron and hole effective masses, respectively. m_0 is the free electron mass.

	Band-gap	Electron affinity	Dielectric constant	Effective mass
Monolayer MoS_2	1.8eV	4.28eV	4.8	m_e=0.5726m_0 m_h=0.6591m_0
Bilayer MoS_2	1.6eV	4.29eV	6.9	m_e=0.5155m_0 m_h=1.039m_0
Monolayer WSe_2	1.64eV	3.53eV	4.5	m_e=0.345m_0 m_h=0.3445m_0
Bilayer WSe_2	1.537eV	3.67eV	6.3	m_e=0.4115m_0 m_h=1.322m_0

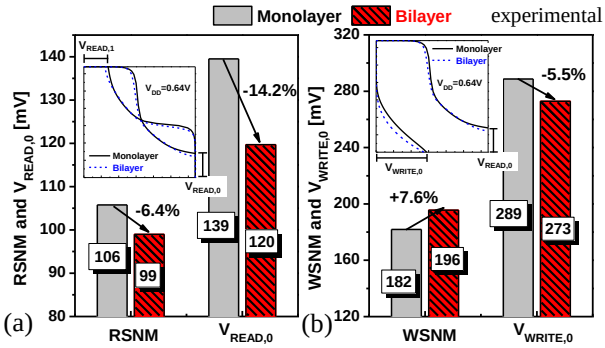

Fig. 3. (a) RSNM and (b) WSNM comparisons of monolayer and bilayer MoS_2-n/WSe_2-p 6T super-threshold SRAM cells at V_{DD}=0.64V.

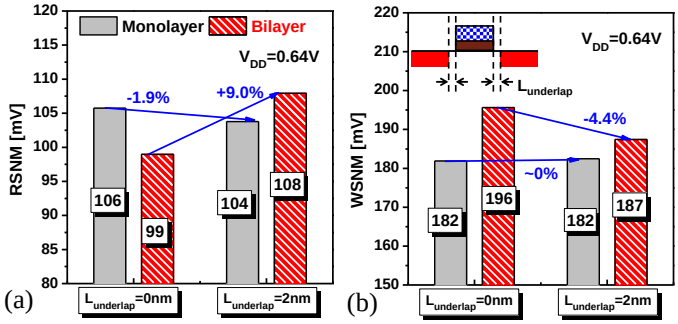

Fig. 4. Impacts of gate-to-source/drain underlap design on (a) RSNM and (b) WSNM of monolayer and bilayer super-threshold SRAM cells at V_{DD}=0.64V.

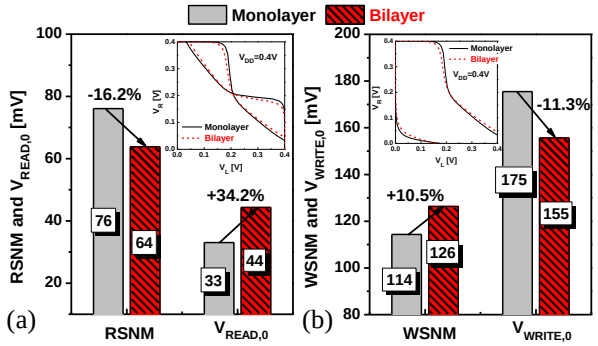

Fig. 5. (a) RSNM and (b) WSNM comparisons of monolayer and bilayer MoS_2-n/WSe_2-p 6T near-threshold SRAM cells at V_{DD}=0.4V.

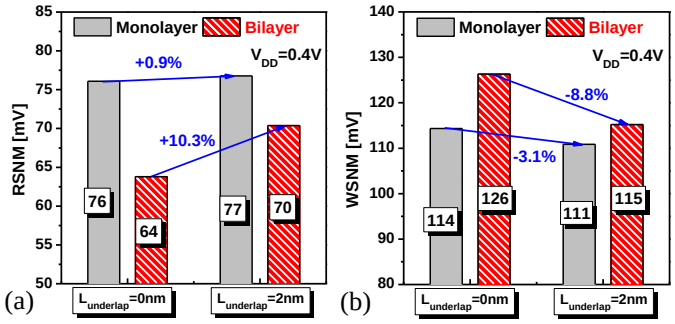

Fig. 6. Impacts of gate-to-source/drain underlap design on (a) RSNM and (b) WSNM of monolayer and bilayer near-threshold SRAM cells at V_{DD}=0.4V.

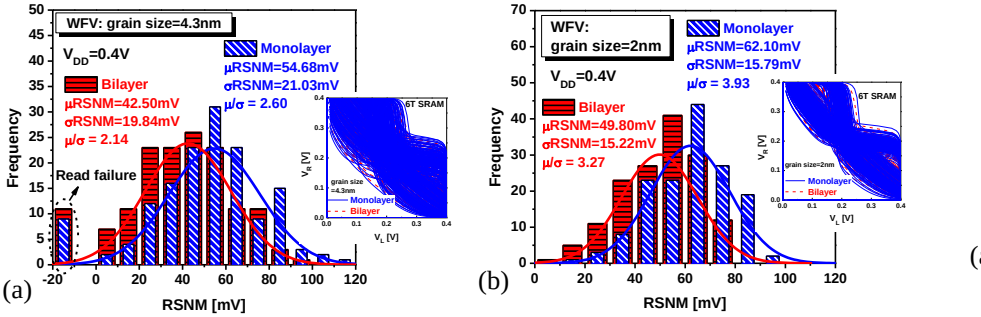

Fig. 7. RSNM variability comparisons for monolayer and bilayer MoS_2-n/WSe_2-p 6T near-threshold SRAM cells considering WFV at V_{DD} = 0.4V with grain sizes = (a) 4.3nm and (b) 2nm.

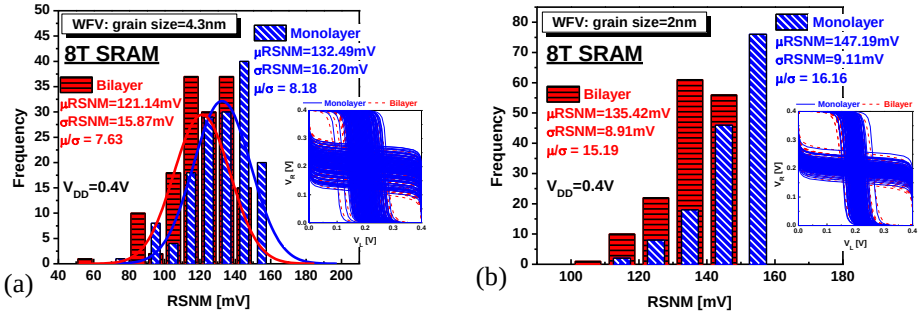

Fig. 8. The significant RSNM variation induced by WFV can be mitigated by using the standard 8T SRAM cell. Grain size = (a) 4.3nm and (b) 2nm. Note the non-Gaussian distribution for grain size = 2nm as it approaches the theoretical limit of RSNM in 8T SRAM cell.

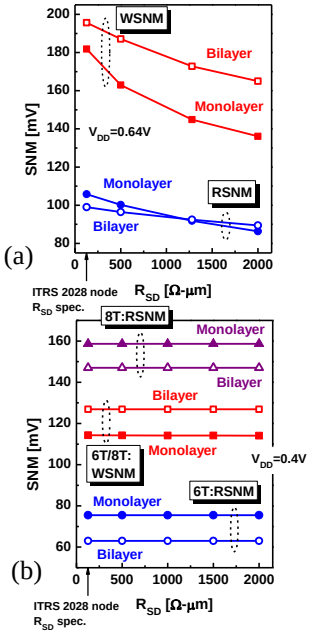

Fig. 9. Impacts of R_{SD} on the stability of monolayer and bilayer SRAM cells at (a) V_{DD}=0.64V and (b) V_{DD}=0.4V. The write operation of the standard 8T SRAM cell is identical to that of 6T SRAM cell.