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Experimental Demonstration of Negative Capacitance epi-Ge/Si FETs with Ferroelectric Hf-based Oxide Gate Stack for Swing Sub-60mV/dec and Hysteresis-Free

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Abstract

The integrating Ge FETs (field-effect transistors) with ferroelectric HfZrOx gate stack for subthreshold swing (SS) < 60 mV/dec and hysteresis-free behavior by negative capacitance (NC) effect is demonstrated experimentally. The capacitance of the semiconductor and ferroelectric film is matched to obtain the no-threshold voltage shift for forward and reverse sweeps without hysteresis. The body factor and modeling are performed to validate the NC effect and optimize the Ge thickness by numerical calculation, respectively. The proposed promising technology in this work is nanoscale feasible with the opportunity to be the candidate for low-power electronics, such as wearable devices, bioelectronics, and IoT (internet of things) applications.

1. Introduction

Beyond the physical limitation of Boltzmann tyranny $2.3k_bT$/decade for MOSFET at room temperature is an emerging issue for sub-7 nm technology node, and the negative capacitance (NC) concept provides a feasible solution [1,2]. In addition, Hf-based dielectric has reported ferroelectric property with suitable dopants [3]-[6]. The nearly equal combination of HfO_x with ZrO_x presents ferroelectric (FE) behaviors and brings the benefit of the negative NC effect for FETs (field-effect transistors). The MFM (metal/ferroelectric/metal) is studied for the ferroelectricity and the corresponding free energy for the internal voltage amplification of NC [7,8]. The FE Hf-based gate stack on Si is validated practically with process compatibility and is beneficial for device scaling down using Moore's law. Recently, ultrathin $HfZrO_x$ (HZO) (<10 nm) by ALD (atomic layer deposition) for Si planar FET and Fin FET exhibits SS<60 mV/dec with the surface potential amplification by the NC effect [9,10]. On the other hand, the ultrathin Ge directly on Si exhibits high hole mobility [11,12]. In this work, FE Hf-based material is integrated with Ge FET to achieve steep SS, high ON, and hysteresis-free behavior; moreover, the theoretic modeling is established for the NC concept.

2. Device Fabrication

A standard 6-inch MOS-based line is employed to this study. A nominally pure Ge layer is directly grown on 150 mm p-type Si substrates at 525°C by UHV-CVD using GeH_4 precursor and H_2 carrier gas, and the Si cap is grown on top of the epi-Ge to passivate and smoothen the surface. The sacrificial Si cap is consumed after the process. The electron mobility of the epi-Ge FET shows higher than Si with (111) orientation (Fig. 1). HZO is grown by ALD directly on epi-Ge/Si substrate. Then, the 120-nm-thick TiN covers the prior insulator layer by a sputtering system sequentially. The diode area is then defined by photolithography and etched by RIE to form the MESA structure. The n+ regions for drain and source are formed. The annealing process for the crystallization of HZO is performed by RTA in an Ar ambient. The schematic diagram and the equivalent circuit of FE-HZO GeFET are shown in Fig. 2.

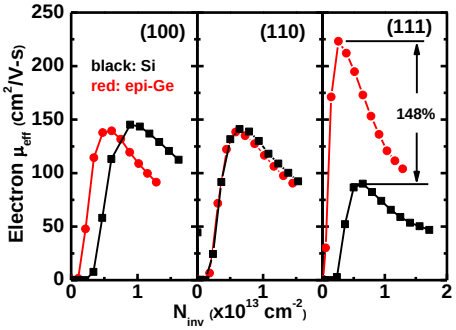

Fig. 1. Electron mobility vs. E-field of epi-Ge/Si NFETs. The peak mobility of epi-Ge (111) shows the highest mobility.

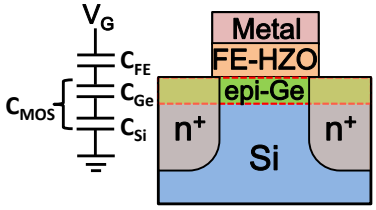

Fig. 2. The schematic diagram and the equivalent circuit of FE-HZO GeFET in this work.

3. Results and Discussion

A physical thickness 6.4 nm FE-HZO (ferroelectric-HZO) and 4 nm Ge on Si by observing cross-sectional HR-TEM are the gate dielectric after annealing (Fig. 3). The GI-XRD is performed after annealing with capping TiN top electrode, and the polycrystalline nature of HZO is confirmed. The Ge and Hf-based oxide with mixture phase signals are observed. To determine the phase of FE-HZO, the crystal structure appears to be a mixture of tetragonal/orthorhombic/cubic phases. The ferroelectricity is believed to be a result of the formation of non-centrosymmetric orthorhombic phase [3][5][6]. The transfer characteristics (I_DV_G) of $Hf_{0.5}Zr_{0.5}O_x$ epi-Ge/Si FET show the ON/OFF ratio ~10^6 and SS= 58mV/dec (Fig. 4). Note that high V_G with high J_G drops I_{DS} off. There is no threshold voltage shift for forward and reverse sweeps with hysteresis-free.

The added C_{Ge} in the equivalent circuit results in the capacitance of epi-Ge/Si MOS close to that of FE-HZO (Fig. 6). In order to validate the NC effect and estimate the behavior by adding C_{Ge}, the modeling is performed with the combination of 2D TCAD and 1D Landau theory (Fig. 5). Note that the quantum effect is also considered in 2D TCAD model. The calculated charge vs. capacitance (Q-C) shows that the two points cross each other between Ge=6nm and FE-HZO (Fig. 6), which indicates the hysteresis behavior. For Ge=2nm, the smallest SS is estimated due to the capacitance close to FE-HZO at lower charges in Q-C (Fig. 6).

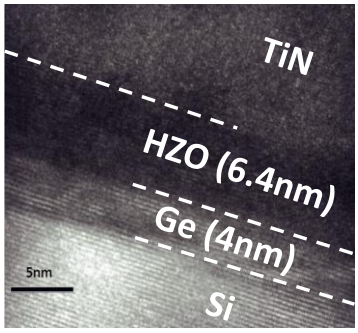

Fig. 3. Cross-sectional HR-TEM of 6.4 nm HZO and 4 nm Ge on Si after annealing.

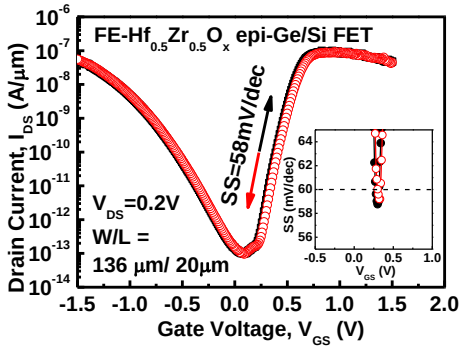

Fig. 4. The measured transfer characteristic (I_DV_G) of FE-HZO Ge/Si FET. I_{ON}/I_{OFF} ~ 10^6 and SS = 58 mV/dec.

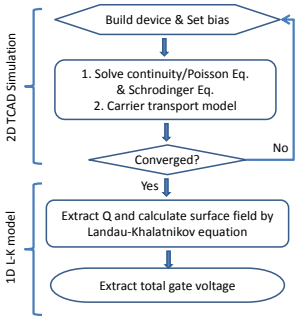

Fig. 5. The modeling procedure of the NC FET. 2D TCAD and 1D Landau theory are used.

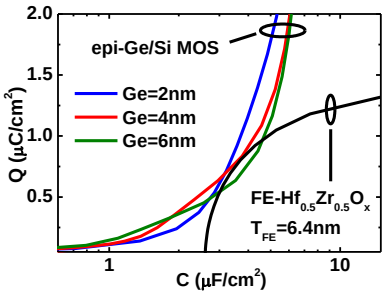

Fig. 6. Calculated Q-C of epi-Ge/Si MOS and FE-HZO with Ge=2, 4, and 6nm. The two points crossing each other indicates the hysteresis behavior.

4. Conclusions

The integration of FE-HZO and Ge FET demonstrates the NC effect for SS < 60 mV/dec and hysteresis-free behavior. The capacitance of the semiconductor and ferroelectricity is matched to obtain the no V_T shift for forward and reverse sweeps without hysteresis. The optimized Ge thickness is obtained by numerical calculation. The proposed technology has the opportunity to be the candidate for low-power electronics, such as wearable devices, bioelectronics, and IoT applications.

Acknowledgements

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