Advantages of Silicon-on-Insulator FETs over FinFETs in Steep Subthreshold Swing Operation in Ferroelectric Gate FETs

Hiroyuki Ota¹, Shinji Migita¹, Junichi Hattori¹, Koichi Fukuda¹, and Akira Toriumi²

¹National Institute of Advanced Industrial Science and Technology
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan
Phone: +81-29-861-3416 E-mail: hi-ota@aist.go.jp
²Department of Materials Engineering the University of Tokyo
7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan

Abstract
In this paper, we discuss the possibility of obtaining steep subthreshold swing using negative capacitance in a fully depleted silicon-on-insulator field-effect transistor (SOI-FET) and FinFET based on technology computer-aided design simulation. Ultrathin buried oxide SOI-FETs are considered as more preferable because they can effectively enable a voltage drop in the ferroelectric layer, which is crucial to attain steep subthreshold swing, through the back electrode.

1. Introduction
The demand for operating energy-efficient large-scale integrated circuits under extremely low voltages has been rapidly increasing. However, the future of downscaling of the supply voltage in conventional MOSFETs seems to be bleak because of the physical limitations of subthreshold swing. FinFETs are considered as more preferable because they can effectively enable a voltage drop in the ferroelectric layer, which is crucial to attain steep subthreshold swing, through the back electrode.

2. Device Simulation

Device structure
Figure 1 shows schematic of the device structures. In this study, planar SOI-FET and FinFET were fabricated on buried oxide (BOX) of various thicknesses.

Stability of the NC
NC states in isolated ferroelectric materials are energetically unstable. Therefore, they should be stabilized by stacking the ferroelectric and paraelectric layers [2, 7]. According to the Landau–Khalatnikov theory, the Helmholtz free energy \( F_F \) per unit volume of a ferroelectric material can be expressed as

\[
F_F = aD^2 + \beta D^4 + \gamma D^6, \tag{1}
\]

where \( D \) is the electric flux density [8], \( \alpha, \beta, \) and \( \gamma \) are the ferroelectric material parameters. In this study, \( \alpha, \beta, \) and \( \gamma \) were chosen so that the remnant polarization and coercive electric field can be 3 \( \mu \)C/cm² and 1 MV/cm respectively, which are typical values of the ferroelectric HfZrO\(_x\) [9, 10]. To stabilize the NC, the total Helmholtz free energy of the gate stack \( F_{total} \) should satisfy \( \partial^2 F_{total}/\partial D^2 > 0 \). This leads to the following constraint on the thickness of the ferroelectric layer \( d_F \):

\[
d_F > 2(3\beta^2/5\gamma) - \alpha\varepsilon_0d_T, \tag{2}
\]

where \( d_T \) is the thickness of SOI (half the thickness of the Fin-channel), and \( \varepsilon_0 \) is the permittivity of silicon. Figure 2 shows the conditions for \( d_T \) and \( d_F \) to stabilize the NC-states. In addition, SS conditions estimated through \( (k_BT/q)(1 + (C_D/C_P)) \), where \( k_B \) is the Boltzmann constant, \( q \) is the elementary charge, \( C_D \) is the depletion capacitance, and \( C_P \) is the ferroelectric gate capacitance and \( T \) is the temperature, were superimposed. For SOI-FETs, \( d_F \) and \( d_{SOI} \) were chosen as 30 and 20 nm respectively, whereas for FinFETs, \( d_F = 15 \) nm and \( d_{SOI} = 10 \) nm (the width of Fin is 20 nm). TCAD simulation was carried out using Silvaco ATLAS™ [11]. The simulation procedure is described in detail in [12].

2. Results and Discussion

Figures 3(a) and 3(b) respectively show the drain current \( I_D \) as a function of the gate voltage \( V_{GS} \) for SOI-FETs and FinFETs on various BOX thicknesses. As shown in Figs. 3(a) and 4, SS of less than 60 mV/decade can be seen in five orders of \( I_D \) under the threshold voltages of SOI-FETs, especially in the case of the ultrathin BOX (UT-BOX). Contrastively, SS values of FinFETs are approximately 60 mV/decade, irrespective of the BOX thickness [Fig. 3(b)].

To elucidate the impact of BOX thickness, potential profiles along the line A-A’ (Fig. 1) in SOI-FETs with 100 nm thick and 2 nm ultrathin BOXs are compared, as shown in Fig.
5(a) \( V_{GS} = 200 \text{ mV}, V_{\text{back}} = 0 \text{ V} \). It should be noted that a voltage drop in the ferroelectric layer in the subthreshold region is indispensable for attaining a subthermal SS. However, a gate voltage drop is observed to predominantly occur in a thick BOX layer.

Figure 5(b) shows a potential profile along the line of B-B’ in the FinFETs with a 2-nm-thick BOX. Figure 3(b) shows that the BOX thickness has negligible impact on SS values of FinFETs. Moreover, as shown in Fig. 5(b), the voltage drops in the ferroelectric layer (in an NC-state) are considerably smaller than those in the ferroelectric layer of SOI-FETs because the ferroelectric layer and the Fin channel are surrounded by the equipotential of the gate electrode in FinFETs. This equipotential suppresses the voltage drop inside the NC layer, and thus hinders reduction of SS.

3. Conclusions

In this paper, the switching performances of SOI-FETs and FinFETs with NC gate insulators based on TCAD simulation were discussed. UT-BOX SOI-FETs were determined to be more preferable for attaining steeper SS than FinFETs. Equipping an electrode to effectively enable a voltage drop in the ferroelectric layer is critical for attaining steep SS in SOI-FETs and FinFETs.

Acknowledgements

This work was supported by CREST, Japan Science and Technology Agency.

References