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Advantages of Silicon-on-Insulator FETs over FinFETs in Steep Subthreshold Swing Operation in Ferroelectric Gate FETs

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Abstract

In this paper, we discuss the possibility of obtaining steep subthreshold swing using negative capacitance in a fully depleted silicon-on-insulator field-effect transistor (SOI-FET) and FinFET based on technology computer-aided design simulation. Ultrathin buried oxide SOI-FETs are considered as more preferable because they can effectively enable a voltage drop in the ferroelectric layer, which is crucial to attain steep subthreshold swing, through the back electrode.

1. Introduction

The demand for operating energy-efficient large-scale integrated circuits under extremely low voltages has been rapidly increasing. However, the future of downscaling of the supply voltage in conventional MOSFETs seems to be bleak because of the physical limitations of subthreshold swing (SS; 60 mV/decade at a room temperature) [1]. Therefore, steep slope transistors, which offer subthermal switching (SS < 60 mV/decade) have been extensively investigated. In particular, ferroelectric gate MOSFETs [2-4] have been gaining considerable attention because a steeper SS has been predicted by harnessing the negative capacitance (NC) state, which was theoretically deduced in an ideal ferroelectric material [2].

So far, several studies have reported successful demonstrations of steep slope-switching in FETs embedding a ferroelectric material such as $HfZrO_x$ [5, 6]. With experimental demonstrations, it is important to design a device to reduce SS effectively.

In this paper, we compare the switching performances of fully depleted silicon-on-insulator FETs (SOI-FETs) and FinFETs based on technology computer-aided design (TCAD) simulation. In general, FinFETs with a paraelectric insulator have reduced SS values than that of SOI-FETs because of better electrostatic control. However, we report, for the first time, that SOI-FETs with an NC gate can attain steeper switching than FinFETs with an NC gate.

2. Device Simulation

Device structure

Figure 1 shows schematic of the device structures. In this study, planar SOI-FET and FinFET were fabricated on buried oxide (BOX) of various thicknesses.

Stability of the NC

NC states in isolated ferroelectric materials are energetically unstable. Therefore, they should be stabilized by stacking the ferroelectric and paraelectric layers [2,7]. According to the Landau–Khalatnikov theory, the Helmholtz free energy F_F per unit volume of a ferroelectric material can be expressed as

$$F_F = \alpha D^2 + \beta D^4 + \gamma D^6, \quad (1)$$

where D is the electric flux density [8]. α, β, and γ are the ferroelectric material parameters. In this study, α, β, and γ were chosen so that the remnant polarization and coercive electric field can be 3 μC/cm^2 and 1 MV/cm respectively, which are typical values of the ferroelectric $HfZrO_x$ [9, 10]. To stabilize the NC, the total Helmholtz free energy of the gate stack F_{total} should satisfy $\partial^2 F_{total}/\partial D^2 > 0$. This leads to the following constraint on the thickness of the ferroelectric layer d_F:

$$d_{FD} > 2[(3\beta^2/5\gamma) - \alpha]\varepsilon_{Si} d_F, \quad (2)$$

where d_{FD} is the thickness of SOI (half the thickness of the Fin-channel), and ε_{Si} is the permittivity of silicon. **Figure 2** shows the conditions for d_{FD} and d_F to stabilize the NC-states. In addition, SS conditions estimated through $(k_B T/q)[1 + (C_D/C_F)]$, where k_B is the Boltzmann constant, q is the elementary charge, C_D is the depletion capacitance, C_F is the ferroelectric gate capacitance and T is the temperature, were superimposed. For SOI-FETs, d_F and d_{FD} were chosen as 30 and 20 nm respectively, whereas for FinFETs, d_F = 15 nm and d_{FD} = 10 nm (the width of Fin is 20 nm). TCAD simulation was carried out using Silvaco ATLAS™ [11]. The simulation procedure is described in detail in [12].

2. Results and Discussion

Figures 3(a) and **3(b)** respectively show the drain current I_D as a function of the gate voltage V_{GS} for SOI-FETs and FinFETs on various BOX thicknesses. As shown in **Figs. 3(a)** and **4**, SS of less than 60 mV/decade can be seen in five orders of I_D under the threshold voltages of SOI-FETs, especially in the case of the ultrathin BOX (UT-BOX). Contrastively, SS values of FinFETs are approximately 60 mV/decade, irrespective of the BOX thickness [**Fig. 3(b)**].

To elucidate the impact of BOX thickness, potential profiles along the line A-A' (**Fig. 1**) in SOI-FETs with 100 nm thick and 2 nm ultrathin BOXs are compared, as shown in **Fig.**

5(a) (V_{GS} = 200 mV, V_{Back} = 0 V). It should be noted that a voltage drop in the ferroelectric layer in the subthreshold region is indispensable for attaining a subthermal SS. However, a gate voltage drop is observed to predominantly occur in a thick BOX layer.

Figure 5(b) shows a potential profile along the line of B-B' in the FinFETs with a 2-nm-thick BOX. **Figure 3(b)** shows that the BOX thickness has negligible impact on SS values of FinFETs. Moreover, as shown in **Fig. 5(b)**, the voltage drops in the ferroelectric layer (in an NC-state) are considerably smaller than those in the ferroelectric layer of SOI-FETs because the ferroelectric layer and the Fin channel are surrounded by the equipotential of the gate electrode in FinFETs. This equipotential suppresses the voltage drop inside the NC layer, and thus hinders reduction of SS.

3. Conclusions

In this paper, the switching performances of SOI-FETs and FinFETs with NC gate insulators based on TCAD simulation were discussed. UT-BOX SOI-FETs were determined to be more preferable for attaining steeper SS than FinFETs. Equipping an electrode to effectively enable a voltage drop in the ferroelectric layer is critical for attaining steep SS in SOI-FETs and FinFETs.

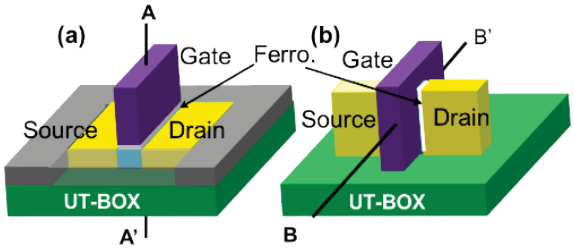


Fig. 1 Schematic of the device structures of (a) SOI-FETs and (b) FinFETs on buried oxide with various thicknesses. The SOI thickness (the Fin width) is 20 nm, and the thickness of the ferroelectric layer for (a) and (b) are 15 and 30 nm, respectively. The height of Fin is 50 nm in (b). The doping concentration of the channel is 1 × 10^{16} cm^{-2} (*p*-type). The work function of the gate electrode is 4.6 eV.

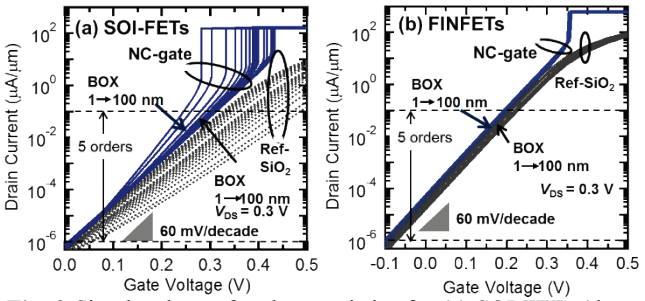
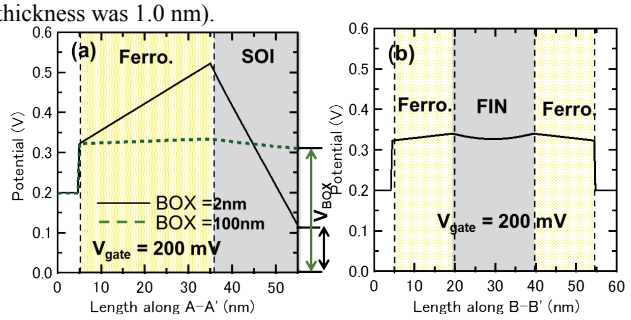


Fig. 3 Simulated transfer characteristics for (a) SOI-FETs (the gate length L_g = 500 nm) and (b) FinFETs (L_g = 100 nm). The thickness of BOX is the parameter. "Ref-SiO_2" indicates simulated transfer characteristics for SOI-FETs and FinFETs with a SiO_2 gate insulator (the thickness was 1.0 nm).



Acknowledgements

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References

[1] H. Fuketa *et al.*, IEDM Tech. Dig., 2011, p. 559.
[2] S. Salahuddin and S. Datta, Nano Lett. 8, 405 (2008).
[3] A. I. Khan *et al.*, IEDM Tech. Dig., 2011, p. 255.
[4] M. Kobayashi *et al.*, VLSI Tech. Dig., 2015, T212.
[5] M. H. Lee *et al.*, IEDM Tech. Dig., 2015, p. 616.
[6] K.-S. Li *et al.*, IEDM Tech. Dig., 2015, p. 620.
[7] J. R. Daniel *et al.*, Nano Lett. 14, 3864 (2014).
[8] M. E. Lines and A. M. Glass, *Principles and Applications of Ferroelectrics and Related Materials* (Oxford University Press, Oxford, U. K., 1979) Chap. 3.
[9] T. S. Böscke *et al.*, IEDM Tech. Dig., p. 548 (2011).
[10] T. Shimizu *et al.*, Jpn. J. Appl. Phys. 53, 09PA04 (2014).
[11] SILVACO International ATLAS User's Manual.
[12] H. Ota *et al.*, Jpn. J. Appl. Phys. 55, 08PD01 (2016).

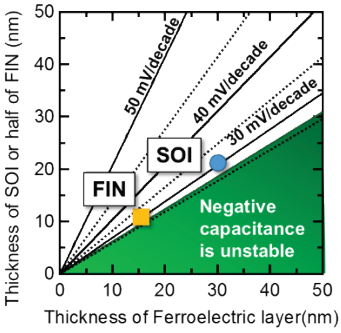

Fig. 2 Thickness of SOI (half the thickness of the Fin) as a function of thickness of the ferroelectric layer to attain steep subthreshold swings. The condition where NC-states are unstable is demarcated in green [see **Eq. (2)**]. The circular and rectangular markers indicate the conditions of TCAD simulation for SOI-FETs and FinFETs, respectively.

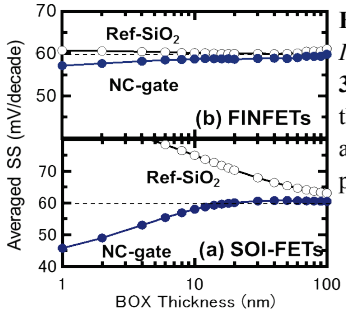

Fig. 4 SS values extracted from I_D-V_{GS} curves shown in **Figs. 3(a)** and **3(b)**. SS shown in those figures is defined as an averaged value between I_D = 1 pA/μm and I_D = 100 nA/μm.

Fig. 5 Potential profiles in a subthreshold condition (V_{GS} = 200 mV, V_{DS} = 300 mV) extracted along the lines of A-A' in SOI-FETs and B-B' in FinFETs. (a) Potential profiles of SOI-FETs with the UT-BOX (2 nm) and the thick BOX (100 nm) are overlaid. The back-bias under the BOX is 0 V. (b) A potential profile of FinFET. This surrounded equipotential suppresses the voltage drop inside the NC-layer.