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New Findings on the Gate-Length Dependence of Subthreshold Swing for Ultra-Thin-Body Negative Capacitance FETs

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Abstract

This work investigates the gate length (Lg) dependence of subthreshold swing (SS) for ultra-thin-body (UTB) Negative-Capacitance-FET (NCFET) by TCAD numerical simulation coupled with 1D Landau equation. Our study indicates that, while the SS of conventional MOSFETs degrades as Lg decreases, the SS of NCFETs improves as gate length decreases because the amplification of gate voltage can be higher in shorter gate length due to stronger drain coupling.

Introduction

NCFET is one of the promising post-CMOS device candidates that may achieve a subthreshold swing smaller than the Boltzmann limit of 60 mV/decade [1]. With similar current transport mechanism to MOSFET [2], NCFET has a layer of ferroelectric material with negative capacitance coating on the gate metal of the bottom MOSFET, and this layer can be viewed as a voltage amplifier. Fig. 1 shows one possible device design for UTB NCFET which can achieve hysteresis-free operation [3,4].

With the scaling of gate length, the degraded subthreshold swing for conventional MOSFETs is a serious problem. In this work, with the aid of TCAD numerical simulation coupled with 1D Landau equation, we investigate the gate-length dependence of SS for UTB NCFETs and report our new findings.

Device Design and Methodology

Fig. 1 shows a schematic sketch and corresponding capacitance model of the UTB NCFET structure in this study. From the capacitance model of the NCFET, we can derive voltage amplification (Av) between V_{MOS} and V_g (Eq. (3)) and the subthreshold swing of NCFET (Eq. (4)). Therefore, there is one design window for the ferroelectric capacitance (C_{FE}) between C_{OX} and the bottom MOSFET capacitance (C_{MOS}): C_{FE} has to be smaller than C_{OX} to achieve subthreshold swing below 60 mV/decade and larger than C_{MOS} to avoid hysteresis [3,4]. As listed in Table I, we use thin buried oxide (T_{BOX}), thin channel thickness (T_{ch}) and thick gate oxide (T_{OX}) to make C_{FE} close to C_{MOS} (Fig. 4(a)) and to get higher Av (Eq. (3)) [3,4]. In other words, C_{MOS} in Eq. (5a) is insensitive to gate bias due to raised depletion capacitance (C_S) and Box capacitance (C_{BOX}) in subthreshold region.

To achieve high Av and hysteresis-free operation, we engineer three ferroelectric parameters including remnant polarization (Pr), coercive field (Ec) and the thickness of the ferroelectric layer (T_{FE}) by considering the minimum of C_{FE} at small Q_{MOS} from the design window with the C_{FE} approximated by Eq. (2). Then, we solve 1D Landau equation [5] to get the Av of the NCFET. The simulation flow is shown in Fig. 2. To achieve a high Av and hysteresis-free operation, we design the NCFET with Pr = 15uC/cm^2, Ec = 1MV/cm^2 and T_{FE} = 20nm so that the minimum of C_{FE} is about 2.89uF/cm^2 at small Q_{MOS}.

Results and Discussion

Fig. 4(b) shows that the SS of the NCFET for Lg = 32nm improves from 109 to 52.7mV/dec due to the Vg amplification by negative capacitance. Fig. 5 shows the I_{ds}-V_g curves of NCFETs with Lg = 5, 8, and 32nm. Fig. 6(a) further shows that the SS of the NCFET improves as Lg decreases while the SS of the bottom UTB MOSFET degrades as Lg decreases (Fig. 7(a)). This is because the Vg amplification is higher as Lg decreases as shown in Fig. 7(b). In order to verify the relation between SS and Lg for NCFETs with other ferroelectric materials, we respectively change the ferroelectric parameters to Pr = 16uC/cm^2 and Ec = 0.9MV/cm^2. Fig. 6(b) further confirms the observed SS vs. Lg relation.

To understand the impact of gate length on Av (Fig. 7(b)), we compare the C_{MOS} versus V_{MOS} characteristics for the bottom UTB MOSFETs with Lg = 32 and 5nm in Fig. 8. It can be seen that due to the drain capacitive coupling, the C_{MOS} for short-channel device (Lg=5nm) in the subthreshold region can be more close to C_{FE} and thus achieve higher Av. In addition, we can use the capacitance model considering drain coupling (Fig. 8(b)) to model a short-channel NCFET. Based on Eq. (5b), we can get the C_d for Lg = 5nm is 7uF/cm^2, which is higher than the extracted C_d for Lg = 32nm, 2uF/cm^2. Although the drain coupling will degrade the ability of gate control for the conventional MOSFET, the drain coupling for the short-channel NCFET improves its subthreshold swing due to higher Av.

Acknowledgement

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References

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[2] Asif I. Khan et al., IEDM, p.11.3.1, 2011.
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[4] C.W. Yeung et al., 3rd Berkeley Symp. E3S, 2013.
[5] C. Hu et al., DRC, 2015.
[6] Synopsis, TCAD Sentaurus Device Manual, 2012.

Table I. Pertinent device parameters for the bottom UTB structure in Fig. 1.

$T_{OX} = 3nm$	$T_{ch} = 1nm$	$T_{BOX} = 1nm$

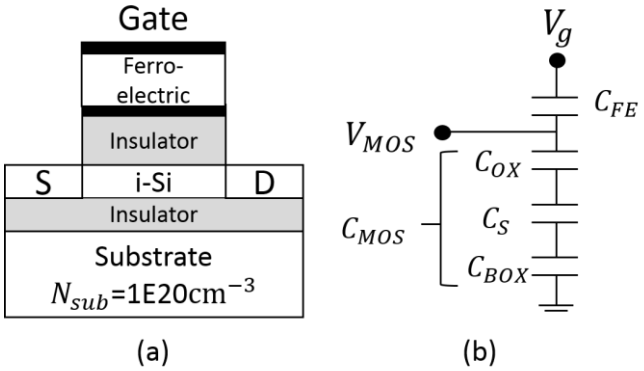

Fig. 1. (a) Schematic sketch of the UTB NCFET [3,4]. (b) Capacitance model of the NCFET.

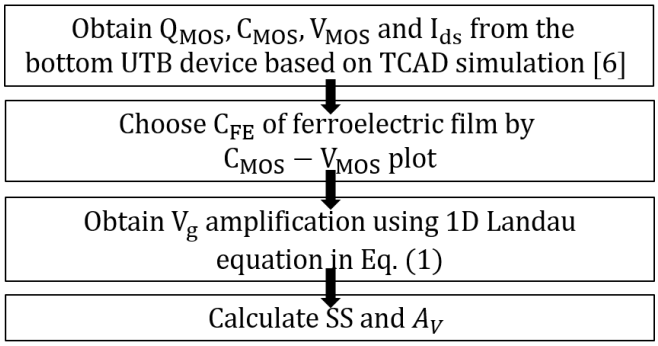

Fig. 2. Numerical simulation flow of NCFET in this work. Q_{MOS} is the gate charge of the UTB device.

$$V_{FE} = V_g - V_{MOS} = -\frac{3\sqrt{3}}{2}\left(\frac{E_C}{P_r}Q_{MOS} - \frac{E_C}{P_r{}^3}Q_{MOS}{}^3\right)T_{FE} \quad (1)$$

$$C_{FE} = \frac{dQ_{MOS}}{dV_{FE}} \approx \frac{2}{3\sqrt{3}}\frac{Pr}{E_C\,T_{FE}} \qquad at\ samll\ Q_{MOS} \quad (2)$$

$$V_g\ amplification = A_V = \frac{\partial V_{MOS}}{\partial V_g} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \quad (3)$$

$$NCFET.SS = UTB.SS \times \frac{1}{A_V} \quad (4a)$$

$$NCFET.SS = 60mV/dec \times \left(1 + \frac{C_{dep}}{C_{OX}} - \frac{C_{dep}}{|C_{FE}|}\right) \quad (4b)$$

$$C_{MOS} = C_{OX} \,||\, (\,C_S \,||\, C_{BOX}) \quad (5a)$$

$$C_{MOS} = C_{OX} \,||\, (\,C_S \,||\, C_{BOX} + C_d\,) \quad (5b)$$

Fig. 3. Pertinent equations used in this work.

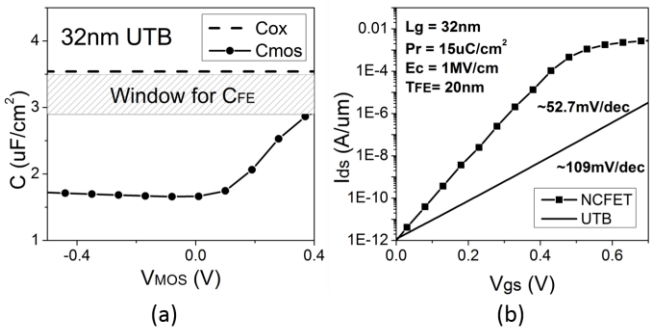

Fig. 4. (a) CV curve of the bottom UTB MOSFET. (b) Id-Vg curves of the NCFET and UTB device with Lg=32nm.

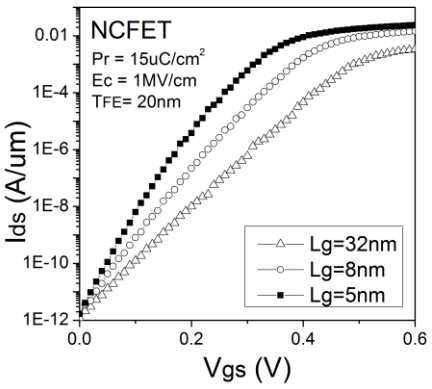

Fig. 5. Id-Vg curves of NCFETs with Lg=16, 5 and 3nm.

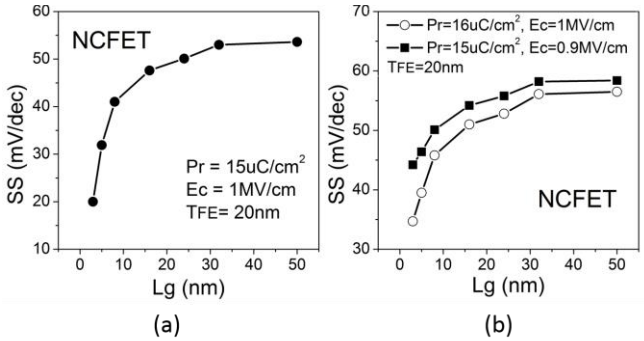

Fig. 6. Improved SS with decreasing Lg for NCFETs with different ferroelectric materials.

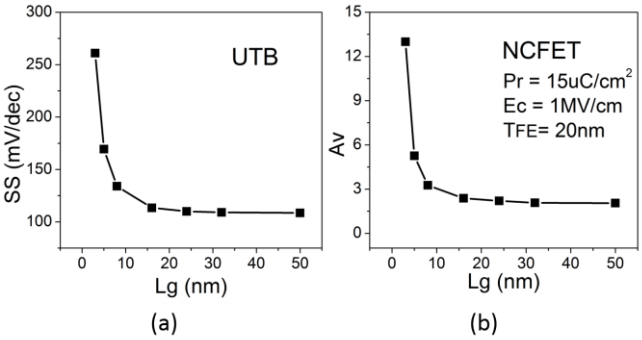

Fig. 7. (a) SS versus Lg for the bottom UTB MOSFET. (b) Av versus Lg for the NCFET. The Av is calculated by Eq. (4a).

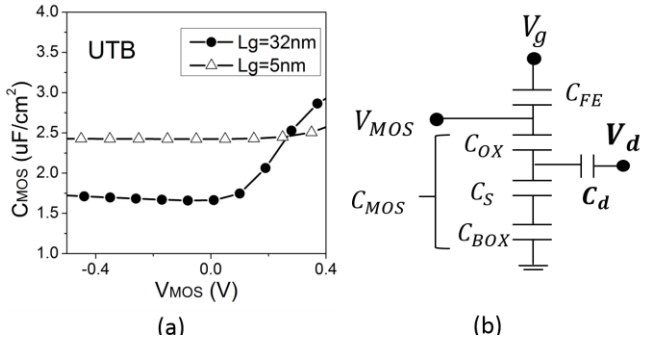

Fig. 8. (a) Comparison of the CV curves for the bottom UTB MOSFETs with Lg=32nm and 5nm. (b) Capacitance model of the short-channel NCFET considering drain coupling.