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Effects of impurity and composition profile steepness on electrical characteristics of GaAsSb/InGaAs hetero-junction vertical TFETs

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Abstract

The electrical properties of vertical GaAsSb/InGaAs TFETs and the physical properties of the source junctions are experimentally characterized. It is found from SIMS and STEM-EDX that the abruptness of the Be profile and the composition gradient width in the GaAsSb/InGaAs source tunnel junctions amounts to be less than 11 nm/dec and 10 nm, respectively. It is found that the experimental *S.S.* values can be well explained by device simulations including the abruptness of both composition and impurity profiles, experimentally obtained.

1. Introduction

Tunnel field effect transistors (TFETs) have widely been studied as promising candidates for steep slope devices[1]. For achieving the high ON current and low leakage current simultaneously, the introduction of hetero structures to source/channel junctions of TFETs is known to be quite effective. From this viewpoint, the source-channel hetero-junctions with type-II (staggered) band alignment are useful for TFETs, allowing us to design the optimal combination of the source and channel materials for reducing the tunnel width (λ) with maintaining large bandgap (E_g) and low leakage current.

Among a variety of type-II hetero-interfaces, $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$, where each layer is lattice matched to InP, can provide relatively low effective tunneling barrier height (E_{b_eff}) of around 0.5 eV with keeping E_g of around 0.7 eV. Recently, GaAsSb/InGaAs TFETs have been experimentally demonstrated[2–5]. However, the *S.S.* values less than 60 mV/dec have not been achieved so far under DC measurements. Here, one of the critical factors to improve the TFET performance the source/channel junction properties. Actually, the effects of the impurity concentration in the source region and the composition profile near the hetero-interfaces on the device characteristics of GaAsSb/InGaAs TFETs have been examined through the tunneling width[3]. However, the quantitative understanding of the relationship of the steepness of the impurity and composition profiles with the device characteristics has not been fully obtained yet. In this paper, we characterize the tunnel junctions of the GaAsSb/InGaAs vertical TFETs by SIMS and STEM-EDX analyses. The effects of the impurity and composition profiles on the electrical properties of GaAsSb/InGaAs TFET are investigated through both experiments and simulations.

2. TFET and Tunnel Heterojunction Characterization

The schematic structure of a GaAsSb/InGaAs vertical TFET and the process flow are shown in Fig. 1. Un-doped $In_{0.53}Ga_{0.47}As$ and Be-doped p^+-$GaAs_{0.51}Sb_{0.49}$ were successively grown on an InP substrate by metal-organic molecular beam epitaxy (MOMBE). Isolation and source region patterning were conducted by wet etching of H_3PO_4:H_2O_2:H_2O (1:1:7). A 10-nm-thick ALD Al_2O_3 was deposited at relatively low temperature of 150 ºC as a gate insulator after the pre-cleaning using an $(NH_4)_2S_x$ solution for 1 min. Then, Ta gate, Ni/Pt source and Au drain contacts were formed.

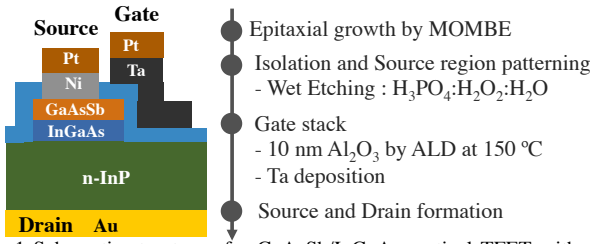

Fig.1 Schematic structure of a GaAsSb/InGaAs vertical TFET with process flow sequences

The impurity and composition depth profiles were performed by secondary ion mass spectrometry (SIMS) by using O^{2+} ions. Fig. 2 (a) shows Be concentration profiles of Be-doped GaAsSb/InGaAs hetero-junction and Be-ion-implanted InGaAs (10 keV, 10^{15} cm^{-2})[6]. The secondary ion intensity of Be in GaAsSb/InGaAs hetero-junction decreased with a slope less than 11 nm/dec at the interface between the two layers, and the slope was much steeper than that of Be-ion-implanted InGaAs (~36 mm/dec)[6]. Fig. 2(b) shows the SIMS profiles of Ga, As, Sb and In in the GaAsSb/InGaAs hetero junction. The In intermixing into GaAsSb was observed because of its surface segregation. In order to clarify the composition ratio in a narrow range of the GaAsSb/InGaAs interface, STEM-EDX analyses were conducted (Fig. 3). The composition gradient width can be estimated to be less than 10 nm. Fig. 4 shows the I_D-V_G characteristics of a fabricated GaAsSb/ InGaAs TFET with channel length/width of 150 nm/100 μm at 297 and 20 K. At 20 K, the minimum *S.S.* value of ~ 80 mV/dec and ON/OFF ratio of ~ 4.5 ×10^4 were obtained at V_D = 50 mV thanks to suppression of the trap-related generation/recombination current in the whole source pn junction. As a result, the characteristics at 20 K can be regarded as the ones determined only by Zener tunneling at the source junction.

3. Analysis of Tunnel Heterojunction dependence

In order to clarify the factors determining the electrical

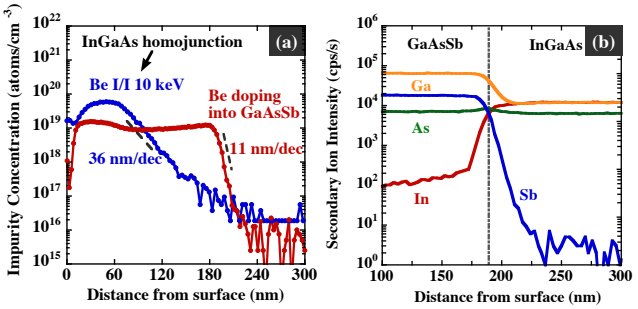

Fig. 2 (a) SIMS profiles of doped Be in GaAsSb layers and implanted Be in InGaAs layer. Steepness of the Be profile in GaAsSb is less than 11nm/dec. (b) SIMS profiles of Ga, As, Sb and In in a GaAsSb/InGaAs hetero junction.

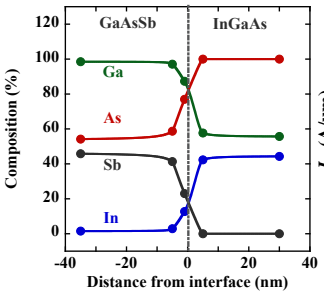

Fig. 3. STEM-EDX analyses of GaAsSb/InGaAs hetero-junction in a narrow range.

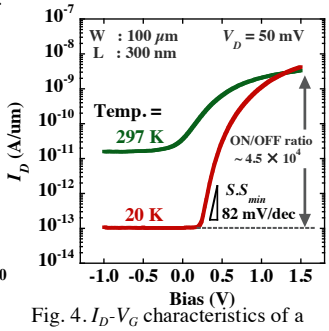

Fig. 4. I_D-V_G characteristics of a GaAsSb/InGaAs TFET at V_D = 50 mV at 297 and 20 K

characteristics of the TFET, the impacts of abruptness of the impurity and composition profiles on electrical characteristics of the GaAsSb/InGaAs TFET were calculated by using a TCAD simulator (Synopsys Sentaurus Device). Here, only the tunneling mechanism was assumed without any other defect-related currents. The simulation structure is shown in Fig. 5(a). The single gate structure was assumed to simulate the present experimental structure. We employed 5-nm-thick SiO_2 as the gate oxides with EOT equivalent to 10-nm-thick Al_2O_3 in the present TFETs. All simulations were carried out at V_D = 50 mV.

In order to study the effects of the source impurity profile near the source/channel junction, the abruptness of the Be concentration near the junction interface was varied from 0 to 5, 10 and 15 nm/dec, as shown in Fig. 5(b), in the simulation. Fig. 6(a) shows the simulated I_D-V_G characteristics of GaAsSb/InGaAs TFETs as a parameter of the abruptness. The experimental result at 20 K was shown at the same time for comparison. As the abruptness is less steep, the ON current and *S.S.* values were degraded. It is found, however, that only doping profile can not accounts for the degradation of the experimental *S.S.* values. Therefore, the effect of the composition profile on device performance was also examined. Here, the experimental composition profile of GaAsSb/InGaAs, shown in Fig. 3, was included in the simulation. Fig. 6(b) shows the *S.S.*-I_D characteristics with and without the composition profile. It is found that the minimum *S.S.* value increases with the graded composition profile, attributed to the increase in the tunneling distance. This fact confirms us the importance of the control of the composition profile in terms of the TFET performance. Fig. 6(c) shows the minimum *S.S.* values of the GaAsSb/InGaAs TFETs with and without the composition profile as a function of the Sb profile abruptness. It is confirmed that the abruptness in both the impurity and composition profiles is important in reducing *S.S.* The experimental minimum *S.S.* value is found to be in agreement with the value simulated with considering both the impurity and composition abruptness. As a consequence, we can conclude that further reduction in *S.S.* values down to lower than 60 mV/dec can be realized by improving the abruptness of both the impurity and composition profiles.

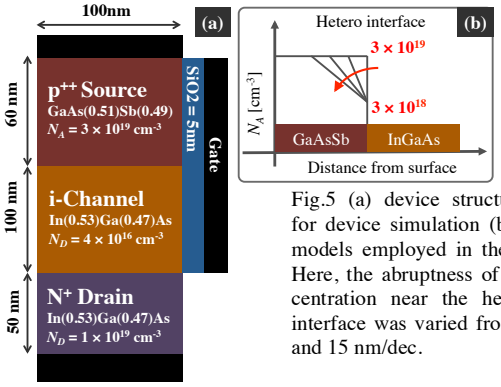

Fig.5 (a) device structure assumed for device simulation (b) Be profile models employed in the simulation. Here, the abruptness of the Be concentration near the hetero-junction interface was varied from 0 to 5, 10 and 15 nm/dec.

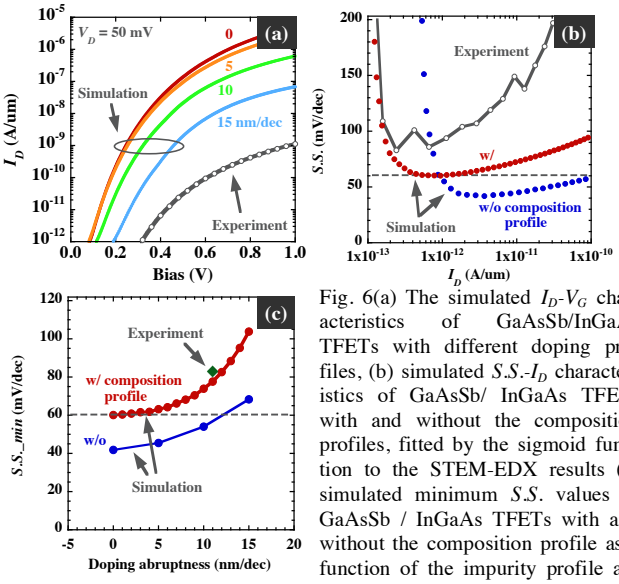

Fig. 6(a) The simulated I_D-V_G characteristics of GaAsSb/InGaAs TFETs with different doping profiles, (b) simulated *S.S.*-I_D characteristics of GaAsSb/ InGaAs TFETs with and without the composition profiles, fitted by the sigmoid function to the STEM-EDX results (c) simulated minimum *S.S.* values of GaAsSb / InGaAs TFETs with and without the composition profile as a function of the impurity profile abruptness.

4. Conclusions

The electrical properties of vertical GaAsSb/InGaAs TFETs and the physical properties of the source junctions have been experimentally characterized. It was found that both the steep composition profile as well as the impurity profile are quite important for obtaining S.S. value of less than 60 mV/dec.

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