A-2-05

InGaAs/Si heterojunction tunnel FET with modulation-doped channel

Katsuhiro Tomioka[1,2], Fumiya Ishizaka[1], Junichi Motohisa[1], Takashi Fukui[1]

[1] Graduate School of Information Science and Technology, and
Research Center for Integrated Quantum Electronics (RCIQE), Hokkaido Univ.
North 13 West 8, Kita-ku, Sapporo 060-0814, Japan
[2] Japan Science and Technology (JST) - PRESTO
4-1-8 Honcho Kawaguchi, Saitama 332-0012, Japan
Phone : +81-11-706-7189, e-mail : tomioka@rciqe.hokudai.ac.jp

Abstract

Tunnel FETs with steep subthreshold-slope have been attracted much attention as one of millivolt switches in future integrated circuits. The device, however, poses inherent issues in low drive current. Here we report on vertical tunnel FETs using InGaAs nanowire/Si hetero-junctions with modulation doped layer. The device demonstrates steep subthreshold-slope (minimum SS ~ 36 mV/dec) turn-on behavior and rapid enhancement of the drive current.

1. Introduction

The main purpose of future electronics such as IoT devices using integrated circuits is realizing low power consumption (long battery life) while enhancing their performance. Simple and difficult task for decreasing the power consumption is to lower supply voltage (V_{dd}) of MOSFETs since the active power of integrated circuits is proportional to the square of the V_{dd} and stand-by power is proportional to the V_{dd} and off-state leakage current (I_{off}). The V_{dd} is determined by the difference in on-state current (I_{on}) with I_{off}, and the subthreshold slope (SS). Therefore, The V_{dd} can be effectively decreased by enhancing the I_{on} under the low bias, lowering the I_{off} by suppressing short-channel effect, and minimizing subthreshold-slope (SS). In this regard, Si-based CMOS technologies are expected to utilize multi-gate structure [1,2], new channel materials [3], and switching mechanism [4]. Moreover, these distinct features should be mutually addressed in extended CMOS technologies and then these technologies should be eventually integrated as a vertical architecture.

The TFETs is a promising switch device for lower the SS because the tunneling transport mechanism can avoid physical limitation of SS in MOSFET (SS ~ 60 mV/dec.). Using TFETs with SS <30 mV/decade would reduce the total power consumption of integrated circuits by over 90% because the reduction in SS lower the V_{dd}. Therefore, various TFETs using Si [5], III-V [6,7], graphene [8] have been investigated and semiconductor nanowires (NWs) have been investigated; However, all had difficulties in attaining sufficient steepness (SS <30 mV/decade) owing to significant challenges such as precise doping techniques to form abrupt tunnel junctions. In this regard, combining Si and III-V materials in one-dimensional (1D) nanostructures could provide a decisive solution to the problem because III-V/Si interfaces formed by integrating III-V NWs on Si have inherently abrupt junctions with band discontinuity [9,10]. Also atomically flat junction using 2D-TMD/p-Ge heterojunction have been reported as tunnel junction [11]. However, TFETs still poses inherent issue in low drive current due to intrinsic higher series resistance.

Here we report on InGaAs NW/Si heterojunction TFET structure with surrounding-gate modulation-doped nanowire channel in order to enhance the drive current. The vertical TFET demonstrated steep SS (SS ~ 36 mV/dec) at room temperature and small DIBL (~16 mV/V). And the drive current of the device offered by the modulation-doped nanowire channel was 1000-times enhancement, to an estimated 3 μA/μmas compared to that of bare InGaAs nanowire-channel.

2. Experimental details

2-1. Formation of InGaAs/InP/InAlAs/InGaAs core-multishell NWs on Si by selective-area growth

The substrate was *p*-type Si(111) with carrier concentration of ~ 5×10^{-18} cm^{-3}. After 20 nm-thick SiO_2 was formed by thermal oxidation, openings were formed using electron beam (EB) lithography and wet etching. $In_{0.7}Ga_{0.3}As$ NWs were grown in low-pressure horizontal MOVPE system. We utilized specific growth sequence to align vertical InGaAs NWs on Si substrate [12]. Tetraethyl-tine (TESn) was used for n-type dopant, and Zn-pulse doping technique [00] was used to make pseudo intrinsic layer as channel region. The NWs were composed of Zn-pulse doped/Si-doped axial junction, whose carrier concentration of the Zn-pulsed region was 5×10^{15} cm^{-3}. As for InP/InAlAs/InGaAs multishell layer, we used lateral-over growth after the formation of the core InGaAs NWs.

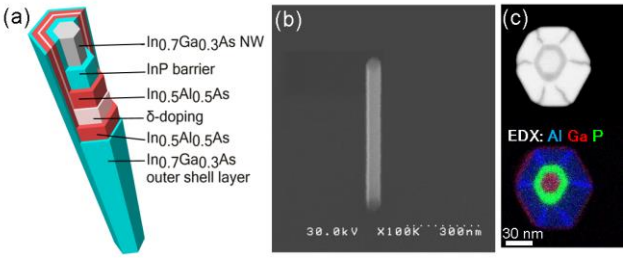

Fig. 1 (a) Illustration of InGaAs/InP/InAlAs/InGaAs core-multishell (CMS) NW growth. (b) 30°-tilted SEM showing growth result of vertical InGaAs CMS NW on Si. (c) HAADF-STEM image (upper panel), and EDX-mapping image showing mixing of Al, Ga, and P atoms (lower panel).

Fig. 1(b) shows the growth results. The NW was 70 nm in total diameter and 1.2 μmin height. The core diameter was 17 nm. EDX profile in Fig. 1(c) exhibits the InP and InAlAs multilayer were formed around the NW-sidewalls. The core InGaAs NW was composed with n^+-InGaAs/Zn-pulse doped InGaAs axial junction. The typical lengths of Zn-pulse doped region and Sn-doped region were 200 nm and 1000 nm, respectively. The carrier concentrations of the n^+-InGaAs and Zn-pulse doped InGaAs were 1.0×10^{19} and 3.5×10^{15} cm^{-3}, respectively.

2-2. Fabrication process for TFET structure.

We fabricated a TFET with a single vertically aligned InGaAs/InP/InAlAs/InGaAs core-multishell (CMS) NW [Fig. 2(a)]. The device processes for the TFET were the same as previously reported [9,10]. First, the NW was covered with 10-nm-thick $Hf_{0.8}Al_{0.2}O_x$ by using atomic-layer deposition. Next, tungsten (W) gate-metal was deposited by RF sputtering and patterned the gate region by wet process. Spin-coated BCB film and etch-back procedure were used to make vertical three-terminal device. As for drain contact, Ni-InGaAs alloy process for the NW [13] and Ni-silicidation were used to form drain/source contact. After removing non-reacted Ni, Ti/Pd/Au multilayer were evaporated as drain and Ni/Au was deposited on backside of *p*-Si to serve as source electrodes.

3. Results and discussion

Figure 2(b) shows representative transfer properties of the InGaAs NW/Si TFET with CMS structure at drain-source voltage (V_{DS}) of 0.25 – 1.00 V. The curve was measured at room temperature. The measured current was normalized using gate-perimeter. Switching behavior with a SS of 36 mV/dec was obtained under reverse bias direction (V_{DS} is positive against *n-i-p* junction). The steep SS region maintained over 3 decade. The dashed line stands for the physical limitation of SS in MOSFET (SS ~ 60 mV/dec.) T The SS of the TFET exhibit steep SS behavior under positive V_{DS}. The ratio of the I_{ON}/I_{OFF} current was over 10^5 at V_{DS} of 0.25 V. The on- and off-state currents were about 3.0×10^{-6} and 1.0×10^{-11} A/μm at V_{DS} = 0.50 V. The threshold voltage, V_T, of the I_{DS} was -0.20 V. Fig. 2(c) show output characteristic of the device indicating the dark Zener current generated at the InGaAs NW/Si heterojunction was modulated by the V_G. The I_{ON} was ~ 3.0 μA/μm at $V_{DS} = V_G - V_T$ = 0.50 V. The DIBL was 16 mV/V indicating that the internal electrical field is applied at tunneling junction regardless of surface potential lowering due to V_{DS}. On the other hand, I_{OFF} due to tunneling leakage was increased at V_{DS} = 1.00 V. This is because that the tunneling from channel to source region was enhanced with increasing V_{DS} owing to narrowing effective gap across the InGaAs/Si.

Figure 2(d) shows the SS with the variation of drain current at V_{DS} = 0.25 V. As compared to the TFET using bare InGaAs NW/Si heterojunction (blue circles), the I60 was increased to 3.0×10^{-9} A/μm and the drive current was enhanced. Moreover, off-state leakage current was slightly increased due to the generation of 2DEG inside the InGaAs NW-channel region.

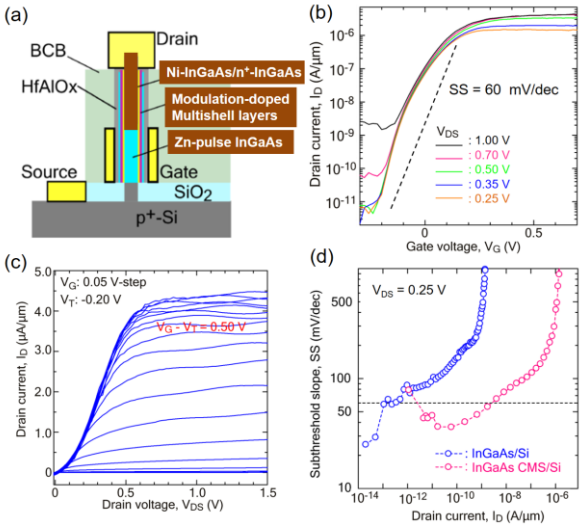

Fig. 2 (a) Illustration of vertical TFET using CMS NW-channel. Gate length (L_G) was 200 nm. Thickness of HfAlO was 10 nm. The NW-length was 1.2 μm. The length of Zn-pulse doped segment was 200 nm. (b) Experimental transfer curve. The dashed curve is physical limitation of SS in MOSFETs. (c) Experimental output property. (d) Subthreshold slope with a variation of I_D at V_{DS} = 0.25 V. Dashed line is physical limitation of MOSFET (SS ~ 60 mV/dec).

Figure 2(c) indicated current-fluctuation under high bias. This is because the thickness fluctuation of multishell layer. More uniform shell layer would improve the performance and it imply the modulation-doped layer contribute to the ON-state current.

4. Conclusions

We have demonstrated current boosting technology using modulation doped NW-channel in the III-V/Si heterojunction TFET structure. The device showed steep SS (~ 36 mV/dec) turn-on behavior and current enhancement which was 1000 times higher than that of the TFETs without the CMS layer. Next issue is to stabilize the drive current under high electrical field and channel-length scaling.

Acknowledgements

This work was funded by JST-PRESTO program and MEXT.

References

[1] I. Ferrain and A. A. Colinge, Nature **479** (2011) 310.
[2] H. Takato *et al*., IEEE Trans. Elec. Dev. **38** (1991) 573.
[3] J. A. del Alamo, Nature **479** (2011) 317.
[4] A. C. Seabaugh, Q. Zhang, Proc. IEEE **98** (2010) 2095.
[5] W-Y. Choi *et al*., IEE Elec. Dev. Lett. **28** (2007) 743.
[6] G. Dewey *et al*., IEEE IEDM Tech. Dig. 785 (2011).
[7] D. Mohata *et al*., IEEE Elec. Dev. Lett. **33** (2012) 1568.
[8] L. Brintnell *et al*., Science **335** (2012) 947.
[9] K. Tomioka and T. Fukui, Appl. Phys. Lett.**98** (2011) 083114.
[10] K. Tomioka *et al*., Nano Lett. **13** (2013) 5822.
[11] D. Sakar *et al*., Nature **526** (2015) 91.
[12] K. Tomioka *et al*., Nature 4**88** (2012) 189.
[13] R. Chen and S. A. Dayeh, Nano Lett., **15** (2015) 3770.