Carrier Transport Analysis of High-performance Poly-Si Nanowire Transistors

Minoru Oda, Kiwamu Sakuma, Yuuichi Kamimuta, and Masumi Saitoh

Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation 800, Yamano-Isshiki-cho, Yokkaichi 512-8550, Japan Phone: +81-59-390-7946 E-mail:minoru2.oda@toshiba.co.jp

Abstract

Impacts of grain boundaries on the electrical performance of Solid Phase Crystallized (SPC) poly-Si transistors are fully investigated. Although S factor decreases as the grain size gets large or the channel size is scaled, the electron/hole mobility shows weak dependences on those. It means that S factor is much affected by grain boundaries, but the mobility is not. The surface carrier density (N_s) and temperature dependence of the mobility indicate that the electron/hole mobility is determined by Coulomb scattering in grains/phonon scattering at low N_s , and by surface roughness scattering/phonon scattering at high N_s , respectively. Suppressing the surface roughness and eliminating defects in grains are essential for further improvement of the mobility of poly-Si transistors.

1. Introduction

High-quality poly-Si is one of the most attracting materials for the promising channel material of BiCS and 3D-stacked-CMOS [1, 2]. Many previous works pointed out that the characteristics of poly-Si transistors are determined by grain boundaries in poly-Si films [2, 3], which cannot be easily eliminated by process optimization. However, it is unclear whether the grain boundaries really dominate all electrical performances or not, especially in scaled poly-Si transistors with large grain size. Then, we have recently shown that these grain boundaries have little influence on the electron/hole mobility while S factor is much affected by them for high-performance poly-Si nanowire transistors fabricated by Advanced SPC process [4]. In this paper, we discuss the correlation between grain boundaries, channel size, S factor and the mobility in order to clarify the influence of grains boundaries on the electrical performances. Then, the details of mobility liming mechanism of poly-Si nanowire transistors is discussed for understanding carrier transport mechanism in poly-Si nanowire transistors.

2. Experimental

The process flow of poly-Si nanowire transistors are shown in Fig. 1. Cross sections of the transistors are also shown. The key processes of Advanced SPC are optimized a-Si deposition, crystallization annealing and poly-Si thinning processes. It was confirmed that the narrowest channel width (W) of about 40 nm and the shortest gate length (L_g) of 130nm was demonstrated. The grain size of poly-Si film was estimated from TEM plan view in this study. The carrier mobility was evaluated from the gradient of R_{on} - L_g plot or Split-CV measurement.

3. Results and Discussion

Grain size distributions of the conventional and Advanced SPC poly-Si film are shown in Fig. 2. The optimized process effectively increases the median grain size from 230 nm up to 800 nm. Figure 3 shows I_d - V_g curves of the conventional and Advanced SPC poly-Si for nFET and pFET. It is evident that Advanced SPC shows steeper subthreshold slope and higher I_{on} than that of conventional one. In fact,

the highest field effect mobility of 192cm²/Vs for Advanced SPC is confirmed among previous SPC poly-Si transistors [5-7]. Channel width dependence of S factor in Fig. 4 indicates that S factor is reduced by channel narrowing and more reduction of S factor is observed for Advanced SPC. This is because channel narrowing effectively decreases the number of defects in the channel and large drop is expected for the larger grain size poly-Si film as shown in the right figure of Fig. 4. Contrary to the behavior of S factor, the electron mobility shows almost no change as a function of the channel width. It suggests that the mobility is no longer limited by scattering at grain boundaries traps. Figure 6 also supports this fact since much variation of the electron mobility is observed for the same grain size poly-Si transistors. In order to search the mobility limiting mechanism, the surface carrier density (N_s) dependence and the temperature dependence of the electron/hole mobility are evaluated as shown in Fig. 8 and 9. It can be seen that Advanced SPC shows much higher mobility than conventional SPC from Fig. 8. Moreover, both the mobility exceeds that of bulk Si with the specific orientation at high N_s . On the other hand, strong mobility degradations at low N_s are confirmed even for Advanced SPC poly-Si compared with bulk Si. This strong degradation is attributed to strong Coulomb scattering. In Fig. 9, the temperature dependence of electron mobility at high N_s is weak. This fact indicates that the dominant scattering mechanism of the electron is surface roughness at high N_s . It can be found that the electron mobility at low N_s is also weak. This weak temperature dependence conflicts with strong Coulomb scattering at low N_s . It suggests that not grain boundaries traps but defects inside grains behave as scattering centers in poly-Si transistors, which would weaken the temperature dependence of the electron mobility. Strong temperature dependence of the hole mobility at high and low N_s is similar to bulk Si in Fig. 9, which means that phonon scattering is dominant in all N_s regime for pFET. Figure 10 shows the summary of the electron mobility limiting mechanism. Conventional SPC poly-Si exhibits much lower mobility in all N_s regime, compared with bulk-Si. This lower mobility results from enhanced Coulomb scattering at low N_s and enhanced surface roughness scattering at high N_s . Advanced SPC improves the crystalline quality of poly-Si films, and can reduce the defects in poly-Si films and surface roughness. Then, much increase of the mobility at each N_s can be realized. For further high performance, elimination of defects inside grains and also suppression of the surface roughness is more needed in addition to Advanced SPC process.

4. Conclusions

High performance poly-Si nanowire transistors, of which the field effect electron mobility is $192 \text{cm}^2/\text{Vs}$, are demonstrated by Advanced SPC process. The detailed investigation clarifies that Coulomb scattering by defects inside grains and surface roughness scattering are dominant for nFET at high N_s and low N_s respectively while phonon scattering for pFET.

References

- [1] H. Tanaka et al., VLSI Tech. Symp., 14 (2007).
- [2] C. -C. Yang et al., IEDM, 410 (2014).
- [3] M. Saitoh et al., VLSI Tech. Symp., 178 (2014).
- [4] M. Oda et al., IEDM, 125 (2015).
- [5] Y. Morimoto et al., J. Electrochem. Soc. 144, 2495 (1997).
- [6] M. Miyasaka et al., Jpn. J. Appl. Phys. 36, 2049 (1997).
- [7] H. C. Lin et al., IEEE Trans. Nanotech. 6, 206 (2007).



Fig. 10. The summary of the electron scattering mechanism in poly-Si transistor.

Fig. 9. Electron and hole mobility vs Ns for conventional and SPC poly-Si transistors with those of (100), (110) bulk Si.