Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp29-30

A-3-03

# On the drain bias dependence of tunnel FETs

Koichi Fukuda, Takahiro Mori, Hidehiro Asai, Junichi Hattori, Wataru Mizubayashi, Yukinori Morita, Hiroshi Fuketa, Shinji Migita, Hiroyuki Ota, Meishoku Masahara, Kazuhiko Endo, Takashi Matsukawa

National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan

**Drain bias dependencies of tunnel FETs are discussed, using measurements of SOI based tunnel FETs in comparisons to device simulations. The physical mechanisms of the dependencies of long channel devices are attributed to the carrier distribution functions determined by source and drain Fermi levels, which are different from DIBLs in MOSFETs. The obtained insights are successfully implemented to our TFET compact model.**

## 1. Introduction

Tunnel FETs (TFETs) are widely studied as the candidates for CMOS transistors especially for low power applications [1]. A TFET switches by using band to band tunneling between its source and channel controlled by the gate to source bias. Drain bias dependencies of TFET $I_D$-$V_G$ characteristics are discussed to clarify the scaling limit of the device [2]. For conventional MOSFETs, these dependencies are attributed to the drain induced barrier lowering (DIBL), but for TFETs they are attributed to so-called drain induced barrier thinning (DIBT).

Authors have fabricated TFETs on the stable silicon technologies [3], and noticed that drain induced $I_D$-$V_G$ shifts are observed especially in low $V_{DS}$ conditions even in long channel TFETs. This long channel drain induced $I_D$-$V_G$ shift is more important than DIBT, because it is more fundamental aspects of TFET physics to be discussed before short channel effects. It is also important to study TFET analog applications. Up to now, physical backgrounds of such long channel $I_D$-$V_G$ shifts are not sufficiently discussed in literatures. In this paper, we compare measurements and device simulations of TFETs, and clarify the origin of the $I_D$-$V_G$ shifts. In addition, we have successfully implemented the mechanisms to our TFET compact model.

## 2. Device Fabrication and Simulation Model

In this study, stable silicon technologies are used to fabricate SOI-based TFETs. The high-K metal-gate stack is applied for the effective oxide thickness of 1.5nm to eliminate the influences of gate tunneling currents. Sources and drains are created by conventional implantation and RTA processes. For device isolation, local oxidation LOCOS technique is used.

TCAD system HyENEXSS [4] is used together with our original band to band tunneling (BTBT) model [5]. In the model, energy band is traced to obtain minimum tunneling path for each simulation mesh points. As shown in Fig.1, the tunneling path length is converted to the effective nonlocal electric field, and applied to Kane's formula. The physical parameters of Kane's BTBT generation rates are obtained from the literature [6].

Important aspects of the BTBT model are explained schematically in Fig.2. Although Kane's generation rates are used, it is widely known that there are cases with not enough valence electrons at the tunnel entrances, or too many electrons occupying the density of states (DOS) at the tunnel exits. These are considered by multiplying DOS occupancy factors (*DOF*) to the generation rates $G_{BTBT}$ as in ref. [7].

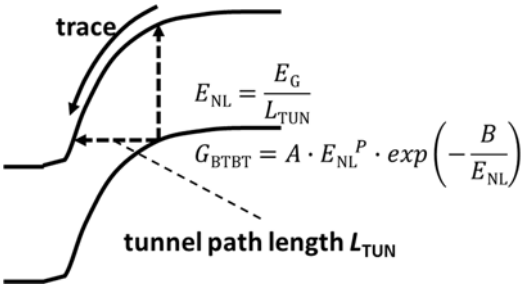


Fig. 1 Concept of the nonlocal BTBT model used in the simulation.

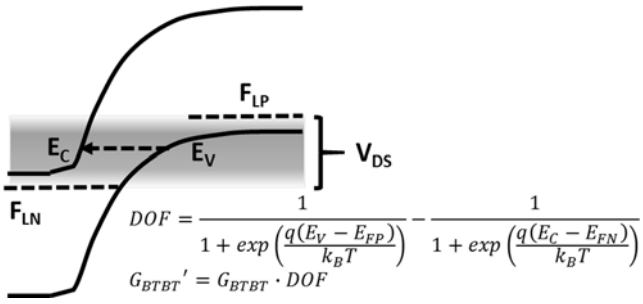


Fig. 2 An image of DOS occupancy factor (*DOF*) used in this work. Carrier tunneling occurs between Fermi levels determined by source to drain biases. The tunneling occurs less near the Fermi levels.

## 3. Results and Discussion

Fig.3 shows $I_D$-$V_G$ curves of the present p-type TFET with gate W/L of 50um/500nm which is sufficiently long to eliminate direct drain potential influences. Here, the drain bias dependencies of each 0.2 volts are measured. The drain dopant concentration is high and no gate-to-drain offset is set, therefore large off currents are observed in region-A. In region-B, current is arising from the parasitic TFET around LOCOS isolation. These two regions are not discussed and we focus on the main curves in the gate biases from -3 to -1.3 volts.

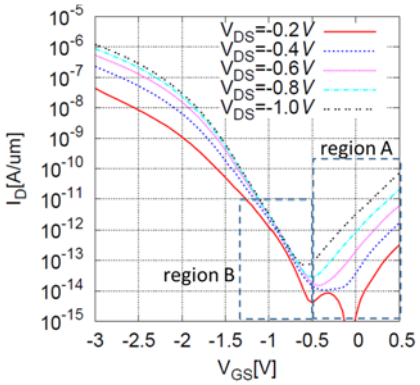


Fig. 3 Measured $I_D$-$V_G$ curves of the fabricated p-type TFET. Region-A is drain originated currents, and region-B is LOCOS originated parasitic currents.

Device simulation results are shown in Fig.4 with two configurations, 1) solid lines with and 2) dashed lines without DOS occupancy considerations. Larger $I_D$-$V_G$ shifts similar to the measurements in Fig.3 are observed in the first case. Fig.5 shows the 2D distribution of the BTBT generation rates (left), and DOS occupancy consideration factors (right) for $V_{DS}$=-0.2V and $V_{GS}$=-1.5V case, evaluated on each tunnel path start points. It is clearly observed that the occupancy factor changes drastically around the peak of the generation rates, which covers only a narrow region in case of $V_{DS}$=-0.2V.

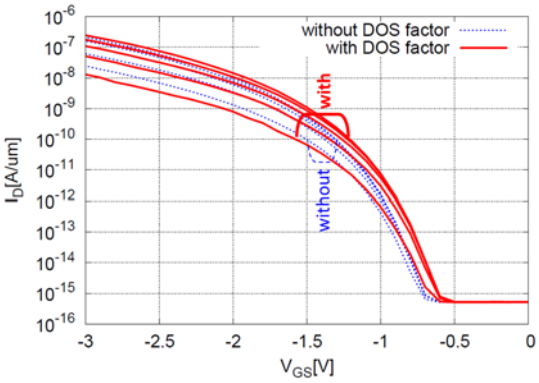


Fig. 4 Simulated $I_D$-$V_G$ curves with (solid lines) and without (dashed lines) DOS occupancy considerations. $V_{DS}$ dependence is enhanced.

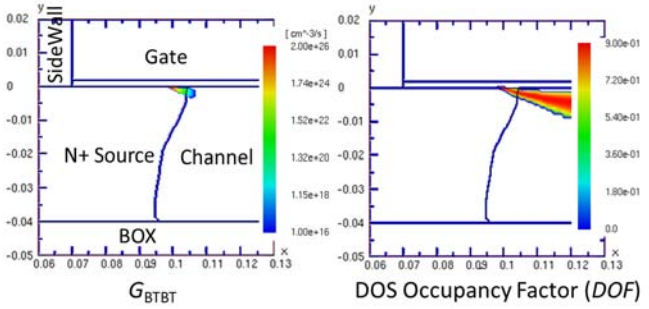


Fig. 5 The distributions of the BTBT generation rates $G_{BTBT}$ (left) and the DOS occupancy factors (*DOF*) multiplied to $G_{BTBT}$ (right) for $V_{DS}$=-0.2V and $V_{GS}$=-1.5V evaluated on each tunnel path start points.

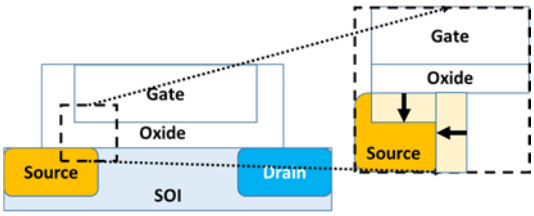


Fig. 6 Schematics of the vertical and the newly introduced lateral depletion around the source junction.

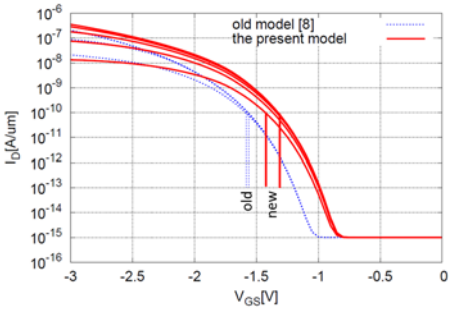


Fig. 7 $I_D$-$V_G$ characteristics calculated by the old (dashed lines) and the present (solid lines) compacted model. $V_{DS}$ dependence is enhanced as shown by vertical guide lines.

Our previous TFET compact model is based on the tunnel path vertical and horizontal paths [8]. To implement the physical aspects of the present drain bias dependencies, it is necessary to add lateral depletion of source junctions arising from gate potential as schematically shown in Fig.6. The $I_D$-$V_G$ curves calculated by SmartSpice circuit simulator [9] with the new model implemented by Verilog-A are shown in Fig.7. The new model explains the $I_D$-$V_G$ shifts successfully.

## 4. Conclusions

Drain bias dependencies of TFET $I_D$-$V_G$ Characteristics are investigated by comparing measurements and device simulations. The $I_D$-$V_G$ shifts observed especially in low $V_{DS}$ conditions are attributed to the DOS occupancy factors even in the long channel TFETs. The basic aspects of the physical background are successfully incorporated to our TFET compact model through the consideration of lateral source depletion. This means more reliable circuit applications are studied by using the proposed compact model.


## Acknowledgements

This work was supported in part by NEDO and by JSPS through FIRST Program initiated by CSTP.


## References


[1] Ionescu, A. M., and H. Riel, Nature 479.7373 (2011) 329-337.
[2] Liu, Lu, D. Mohata, and S. Datta, TED 59.4 (2012) 902-908.
[3] Mori, Takahiro, et al., APEX 7.2 (2014) 024201.
[4] HyENEXSS ver5.5.
[5] Fukuda, Koichi, et al., IWCE IEEE, 2014.
[6] Kao, Kuo-Hsing, et al., TED, IEEE on 59.2 (2012) 292-301.
[7] De Michielis, Luca, et al., EDL, IEEE 34.6 (2013) 726-728.
[8] Fukuda, Koichi, et al., JAP 114.14 (2013) 144512.
[9] SmartSpice, SILVACO, Inc.