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InGaAs-on-Si(Ge) 3D Monolithic Integration for CMOS and More-than-Moore Technologies

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Abstract

3D Monolithic (3DM) integration can provide both density scaling benefits and the possibility to stack independently optimized layers at transistor level. However, top layer thermal budget poses a considerable challenge in such a technology. Due to its inherently low process temperature, InGaAs is well-suited to be used as the top layer channel material. Therefore, InGaAs has the potential to enable both low voltage-high performance advanced CMOS, as well as high-frequency device for RF/mixed-signal applications. In this regard, we show here our recent progress in InGaAs-on-SiGe 3D Monolithic technology, demonstrating state-of-the art device integration on both levels, DC and RF characterization top layer InGaAs nFETs and integrated inverters with sub-50 nm L_g down to V_{DD} = 0.25 V.

1. Introduction

3D Monolithic (3DM) integration is attracting much attention owing to density scaling benefits and the potential to stack independently optimized multifunctional layers at transistor level [1]. Typical Si MOSFET process has high thermal budget, requiring development of low temperature top layer Si/SiGe process for a 3DM scheme and thus presents challenges to obtain high-performance MOSFETs. On the other hand, the InGaAs MOSFET processing thermal budget is significantly lower, making it well-suited to be used as the top layer channel material [2, 3]. Moreover, InGaAs also has higher mobility which enables high performance at lower voltages and is an excellent channel material for high-frequency devices enabling very high cut-off frequency. This aspect is of great interest as it can enable a truly multifunctional 3D monolithic integration scheme. On one hand, InGaAs nFETs on top of Si/SiGe FETs can allow higher performance hybrid CMOS [3] and on the other, high frequency InGaAs RF-FETs can benefit from closely integrated CMOS circuits [4]. As a step towards such a multi-functional 3D monolithic integration, here, we show DC and RF characteristics of InGaAs nFETs fabricated with RMG process on top of SiGe-OI finFETs. A cut-off frequency of 16.4 GHz for gate length (L_g) of 120 nm is obtained. We also show integrated inverters with sub-50 nm L_g down to V_{DD} = 0.25 V in the same stack. Robustness of the technology is demonstrated by the fact that impact on the bottom pFET performance is negligible, despite the top nFET RMG process featuring a self-aligned raised source drain epitaxy (with relatively high thermal budget).

2. Device Integration

The 3DM process flow is described in detail in ref. (3). Firstly, bottom layer SiGe-OI fin pFETs are fabricated with a process described in ref [5]. After the silicidation step of SiGe-OI finFET process, the inter-layer oxide is deposited and CMP planarization is carried out. The InGaAs layer is transferred on to this oxide with direct wafer bonding from InP donor wafers [6]. InGaAs nFET fabrication is then performed with the RMG process described in [7]. Finally, oxide encapsulation is deposited and contact holes are opened and metallization is completed. The schematic of the 3DM stack is shown in fig 1.

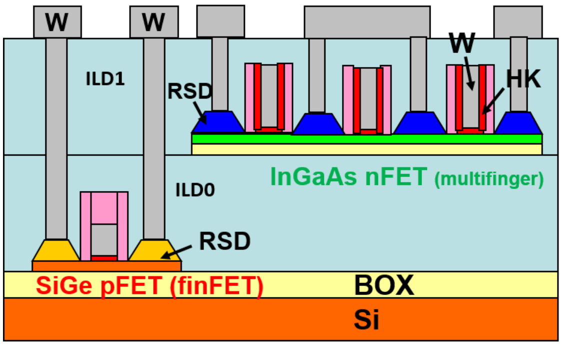

Fig. 1. Schematic the InGaAs-on-SiGe 3DM stack showing nFETs on top of SiGe finFETs.

3. Electrical Characterization

DC characteristics and circuits

Figure 2 shows the DC I_d - V_g characteristics of top layer InGaAs nFET with L_g = 70 nm, demonstrating competitive DC performance after the 3DM fabrication.

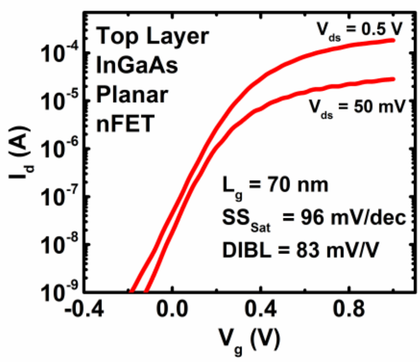

Fig. 2: I_d - V_g of InGaAs planar nFET on the top layer. The device features RMG, which yields very good electrostatics (SS_{sat} = 96 mV/dec, DIBL = 83 mV/V @ L_g = 70 nm).

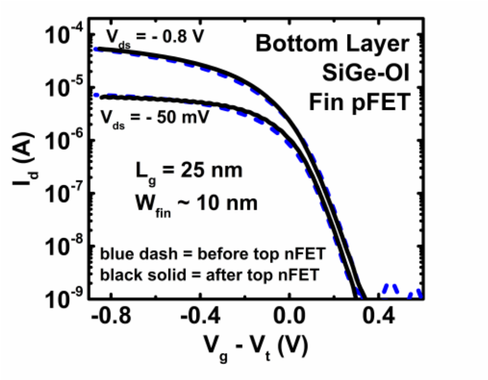

Fig. 3: I_d - V_g of SiGe-OI fin pFET before and after top nFET fabrication. Very similar I_{dsat} is obtained without degradation of electrostatics after top nFET fabrication.

Figure 3 shows comparison of bottom SiGe-OI pFET I_d-V_g before and after top nFET fabrication. Nearly identical I_{dsat} is obtained post-nFET fabrication, indicating negligible impact on pFET silicide. The electrostatics of the device has very minimal change, demonstrating low impact on the gate oxide and source/drain doping profile. This shows the robustness of the process and demonstrates the potential to achieve optimized performance on both, top-nFET and bottom-pFET layers.

Figure 4 shows the the voltage transfer characteristics (VTC) of scaled 3D inverters with nFET L_g = 80 nm (with pFET L_g ~ 30 nm) and L_g ~ 30 nm (for both nFET and pFET). Well-behaved transitions are obtained down to V_{DD} = 0.25 V, demonstrating that an optimized low-voltage CMOS can be achieved with InGaAs-on-SiGe 3DM technology.

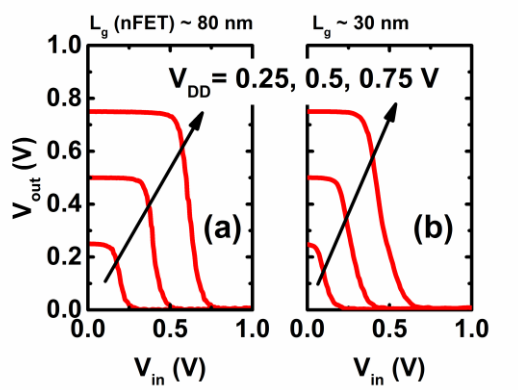

Fig. 4: Voltage transfer characteristics (VTC) of 3DM inverter. Well behaved characteristics are observed down to V_{DD} = 0.25 V owing to independent optimization of top InGaAs nFET and bottom SiGe-OI pFET. In (a) L_g ~ 80 nm in nFET and ~30 nm in pFET, while in (b) L_g ~ 30 nm in both nFET and pFET.

RF characteristics of top layer InGaAs nFETs

The top layer InGaAs nFETs used for RF characterization feature multi-finger gate structure [8] and have a gate-contact spacing of 100 nm. Multifinger gate layout allows lowering the gate-resistance. The measured current gain (after on-chip de-embedding) for a nFET with L_g = 120 nm and 10 gate fingers is shown in fig. 5. A cut-off frequency (F_t) of 16.4 GHz is obtained. Figure 6 shows cut-off frequency vs. gate length. As expected cut-off frequency is observed to increase with lower L_g. Further optimization of layout and device design would allow for higher F_t.

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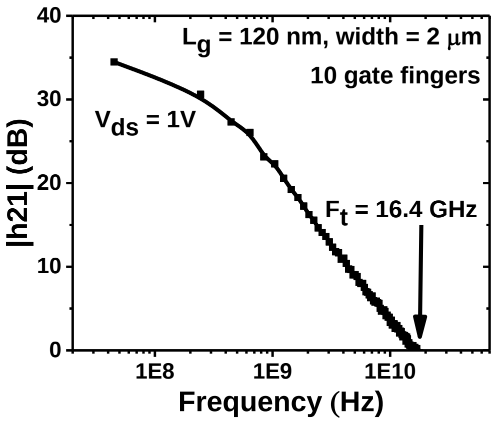

Fig. 5. Measured current gain (|h21|) vs. frequency for a InGaAs nFET (top layer) with L_g = 120 nm and 10 parallel gate fingers. Cut-off frequency (F_t) of 16.4 GHz is obtained for V_{ds} = 1V.

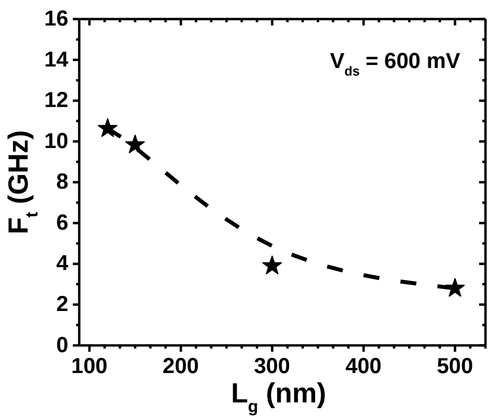

Fig. 6. Cut-off frequency vs. gate length (L_g) for top InGaAs nFETs for V_{ds} = 600 mV.

4. Conclusions

A robust InGaAs-on-Si(Ge) 3D Monolithic integration scheme is demonstrated that allows low voltage high-performance CMOS circuits as well RF-over-CMOS circuits. Owing to inherent benefits of low thermal budget and high mobility InGaAs as top layer enables optimized performance at both layers. Thus building blocks for a high performance, multi-functional 3D Monolithic technology is demonstrated.

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