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Reliability Analysis for Monolithic 3D UTB GeOI and SOI 6T SRAM Cells considering Interlayer Coupling

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Abstract

This paper investigates the impacts of NBTI and PBTI on the stability and performance of UTB GeOI and SOI 6T SRAM cells integrated in monolithic 3D scheme with interlayer coupling. The worst case stress scenarios for read and write operations are analyzed. The optimized monolithic 3D UTB GeOI SRAM with the pull-down NFET tier stacked over the pull-up PFET tier and under forward PFET back-gate bias shows improvements in read stability and cell read-access time compared with the 2D UTB GeOI SRAM. Moreover, the optimized monolithic 3D UTB GeOI SRAM can mitigate the temporal degradations in stability and performance due to BTI stress because the BTI induced threshold voltage degradations can be suppressed by interlayer coupling in monolithic 3D scheme.

Introduction

Ultra-thin-body (UTB) GeOI MOSFET has been proposed as a promising device architecture [1-2] due to its better control of short-channel effects and larger current drive due to higher mobility. Monolithic 3D integration, which sequentially fabricates multiple active layers with dense inter-tier vias, enables the full use of the third dimension [3-4]. Negative and positive bias temperature instabilities (NBTI (for PFET) and PBTI (for NFET)) have become major reliability concerns as they weaken MOSFETs over time [5], resulting in temporal degradations in the stability and performance of the SRAM cells [6]. Several studies have investigated the BTI reliability in Ge MOSFETs. The Si-passivated Ge devices with HfO_2/SiO_2 gate stack show less NBTI degradation than the Si counterparts [7] because there is less hole trapping in the dielectric of the Ge device due to its larger valence band offset. The PBTI degradation of the Ge devices is more severe than the Si counterparts [7]. This may attribute to the lower processing temperature during device fabrication, which results in larger amount of electron traps in the dielectric for the high-k Ge MOSFETs.

In this paper, for the first time, we focus on the impacts of aging effects on the monolithic 3D 6T SRAM cells using UTB GeOI and SOI MOSFETs, respectively, considering interlayer coupling. The impacts of BTI reliability on the read static noise margin (RSNM), write static noise margin (WSNM), cell read-access time and time-to-write are analyzed.

Device Design and Simulation Methodology

Fig. 1 shows the tier combination of top/bottom tiers = NFET/PFET. Using transistor-level TCAD mixed-mode simulations [8], vertical coupling through interlayer dielectric are considered to optimize the physical layouts of monolithic 3D SRAM cells. For comparison, we utilize dual back-gate biases (V_{bg}=0V and V_{dd} for NFET and PFET, respectively) as the base case for planar 2D SRAM cell. For 3D SRAM cell, the V_{bg} of bottom PFET transistor is V_{dd} if not otherwise stated. The UTB MOSFETs used in this study has 25 nm gate length (L_g), 5nm channel thickness (T_{ch}), EOT=0.7 nm with high-k gate dielectric (HfO_2, permittivity=22), and T_{BOX} (T_{ILD})=10 nm. Channel doping concentration (N_{ch})=1E16 cm^{-3}, and source/drain doping concentration (N_{sd})=5.5E19 cm^{-3} for GeOI and 1E20 cm^{-3} for SOI MOSFETs, respectively. Reaction-diffusion model is used to calibrate the experimental data of V_{th} drift due to NBTI/PBTI in Ge MOSFETs [9]. With thin T_{ILD} and significant interlayer coupling, the gate voltages of bottom-tier transistors serve as the V_{bg} of upper-tier devices, thus enabling the designs and optimizations for monolithic 3D SRAM cells. Furthermore, due to thin (10nm) buried oxide (BOX), the interlayer coupling from the gate of bottom-tier transistors is much stronger than other fringing electric fields, such as those from inter-tier vias, V_{dd} or GND lines.

Interlayer Coupling of Monolithic 3D SRAMs

The UTB GeOI and SOI MOSFETs are designed to have the same V_{th} (= 0.2V), and the 6T SRAM cells are analyzed using TCAD mixed-mode simulations. Fig. 2 shows the definitions of RSNM and WSNM, and the worst BTI stress scenario for 6T SRAM. Fig. 3 shows the RSNM comparisons among 2D planar SRAM and various monolithic 3D SRAM cells with UTB GeOI and SOI MOSFETs, respectively. In Fig. 3, the (N/P)-tier PD/PU design(V_{bg_PMOS}=0V), which stacks pull-down (PD) NFET over the bottom-tier pull-up (PU) PFET and uses global/forward bottom back-gate bias, exhibits largest RSNM over other cells. This is because in PD/PU(V_{bg_PMOS}=0V) monolithic 3D SRAM, during read operation, PD with forward back-gate bias reduces read disturb, and PU(V_{bg}=0V) with forward back-gate bias increases the trip voltage, thus improving the RSNM. On the other hand, for PG/PU layout stacking pass-gate (PG) NFET over PU PFET, PG with forward back-gate bias during read operation increases read disturb, thus showing the smallest RSNM. For PG/PU layout, during write operation, PG with forward back-gate bias coupling from the bottom layer PU device becomes stronger, thus increasing WSNM as shown in Fig. 4. Fig. 5 compares the cell read-access time, defined as the time required for bit-line differential voltage to reach 10% of V_{dd}, for planar 2D and 3D cells in (N/P)-tier configuration. As can be seen, the (N/P)-tier 3D SRAM design increases the read current due to stronger upper-tier PD or PG transistors and improves the read performance over the 2D design. Besides, UTB GeOI SRAM cells show smaller cell read-access time than the SOI counterparts due to its higher mobility. The cell time-to-write is defined as the time from the 50% activation of the word-line to the time when the voltages of two cell storage nodes cross each other. For PG/PU and PD/PU with PG/VL(VR) monolithic 3D SRAM cells, due to interlayer coupling from the bottom layer, the upper PG device with forward back-gate bias becomes stronger, thus improving the cell time-to-write as shown in Fig. 6.

BTI Reliability of Monolithic 3D SRAMs

In this paper, worst case static stress pattern (only PR with NBTI and NL with PBTI) is considered as shown in Fig. 2. Under the worst case scenario for read stability, the threshold voltages of NL and PR are increased due to PBTI and NBTI, which increases the read disturb voltage on the VL node, and reduces the trip voltage of the PR-NR inverter, making it easier for the cell to flip during read operation, thus reducing the RSNM. Fig. 7 shows the NBTI and PBTI induced V_{th} shift for UTB GeOI and SOI MOSFETs with various back-gate bias (V_{bs}). As can be seen, UTB GeOI MOSFETs show smaller NBTI and larger PBTI degradations than the UTB SOI MOSFETs. It has been shown that the reverse back-gate bias would increase BTI induced V_{th} shift, while forward back-bias would reduce the BTI degradations. As can be seen in Fig. 7, UTB SOI PFET with forward back-gate bias (V_{bs} = -1V) exhibits smaller V_{th} shift than that with V_{bs}=0V. However, for UTB GeOI PFET with V_{bs}=-1V, forward back-gate bias causes slightly reduction in V_{th} shift due to its larger valence band offset. For both UTB GeOI and SOI NFETs with V_{bs}= 1V, forward back-gate bias reduces the V_{th} shift due to PBTI by 13.4mV and 14.9mV, respectively, as shown in Fig. 7.

Fig. 8 shows the impacts of BTI stress on the RSNM of GeOI and SOI SRAM cells with 2D and various 3D layouts. For UTB GeOI (SOI) SRAMs, PD/PU(V_{bg_PMOS}=0V) 3D SRAM cells show 63mV (43mV) RSNM degradations due to BTI stress; while 2D GeOI (SOI) SRAM cells show 80mV (61mV) RSNM degradations. This is because for PD/PU(V_{bg_PMOS}=0V) 3D SRAM cells during read operation, both PD and PU devices with forward back-gate bias suffer less BTI degradations. In other words, monolithic 3D SRAM cell can mitigate the temporal read stability degradations due to BTI stress. WSNM only degrades slightly due to BTI stress for both GeOI and SOI SRAM cells as shown in Fig. 9. Fig. 10 shows that the cell read-access time degradation due to BTI stress is larger in 2D planar SRAM than in monolithic 3D SRAM cell for both GeOI and SOI SRAMs. The read current is determined by the current through PG and PD transistors stack. For PD/PU(V_{bg_PMOS}=0V) 3D SRAM cells during read operation, PD device with forward back-gate bias suffers less BTI degradation, thus exhibiting smaller cell read-access time degradations due to BTI compared with the 2D cell. Fig. 11 shows the BTI induced cell time-to-write degradations are comparable among 2D and 3D SRAM cells for both GeOI and SOI SRAMs.

In summary, the optimized monolithic 3D SRAM cell with interlayer coupling shows better stability and mitigates the temporal degradations in RSNM and read access time due to BTI reliability.

Acknowledgement

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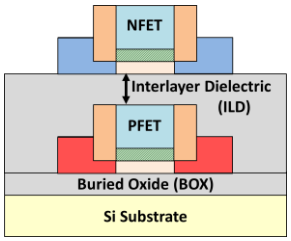

Fig. 1. Schematic view of 3D monolithic stacking with the electrical coupling through the interlayer dielectric (ILD) between top-tier NFET and bottom-tier PFET for UTB GeOI and SOI MOSFETs.

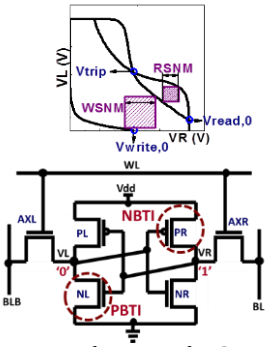

Fig. 2. Definitions of RSNM and WSNM. Worst stress scenario for 6T SRAM cell (only PR and NL suffer from NBTI and PBTI, respectively).

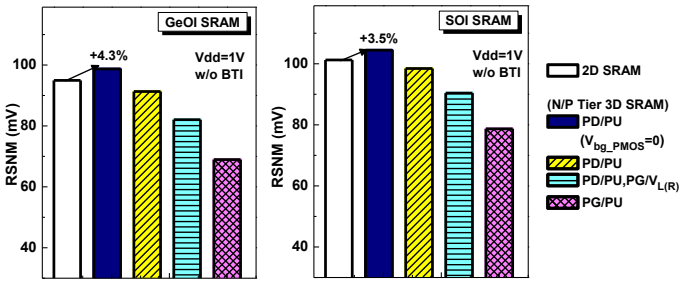

Fig. 3. RSNM comparisons of (a) 6T UTB GeOI SRAM cells and (b) 6T UTB SOI SRAM cells with planar 2D and monolithic 3D design. Vth of UTB GeOI and SOI devices are 0.2V. (PD: pull-down transistor; PU: pull-up transistor; PG: pass-gate transistor; VL/VR: voltages at the cell storage nodes.)

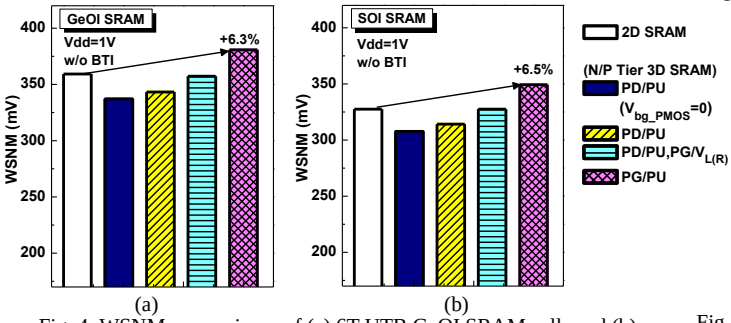

Fig. 4. WSNM comparisons of (a) 6T UTB GeOI SRAM cells and (b) 6T UTB SOI SRAM cells with planar 2D and monolithic 3D design.

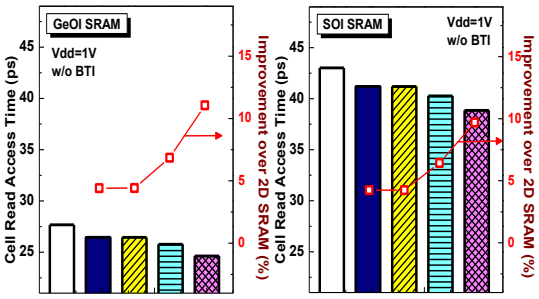

Fig. 5. Cell read-access time comparisons of 6T UTB GeOI and SOI SRAM cells with planar 2D and monolithic 3D design.

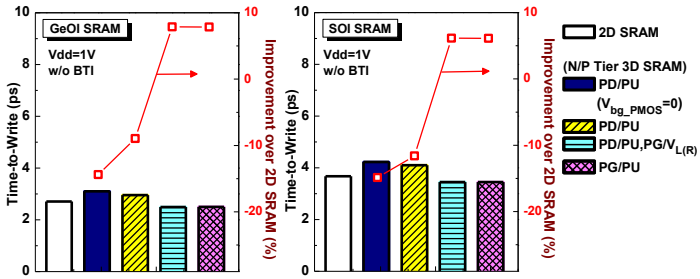

Fig. 6. Time-to-Write comparisons of 6T UTB GeOI and SOI SRAM cells with planar 2D and monolithic 3D design.

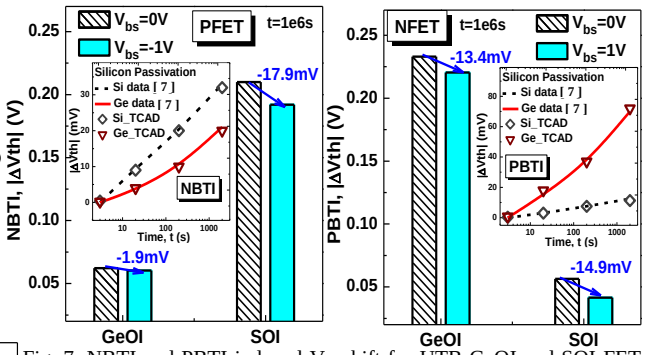

Fig. 7. NBTI and PBTI induced V_{th} shift for UTB GeOI and SOI FETs with V_{bs}=0V and forward back-gate bias (-1V for PFET, and 1V for NFET). Insets show calibration results of the BTI model with the experimental NBTI/PBTI data

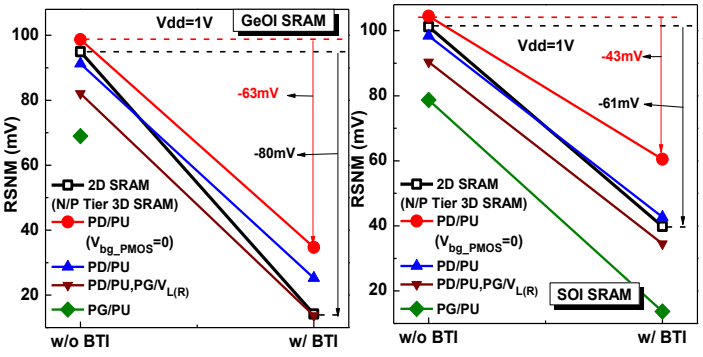

Fig. 8. Impact of BTI stress (t = 1e6s) on the RSNM of 2D and various 3D UTB GeOI and SOI SRAM cells, respectively. The PD/PU(V_{bg_PMOS}=0) shows smaller RSNM degradation compared to the 2D SRAM.

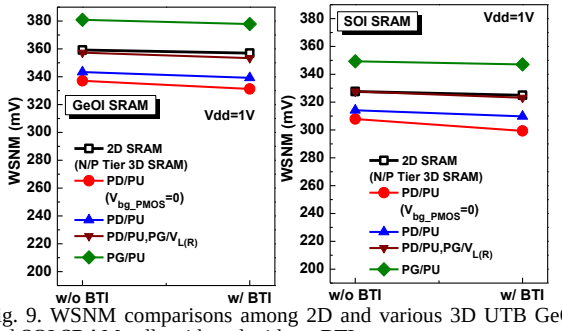

Fig. 9. WSNM comparisons among 2D and various 3D UTB GeOI and SOI SRAM cells with and without BTI stress.

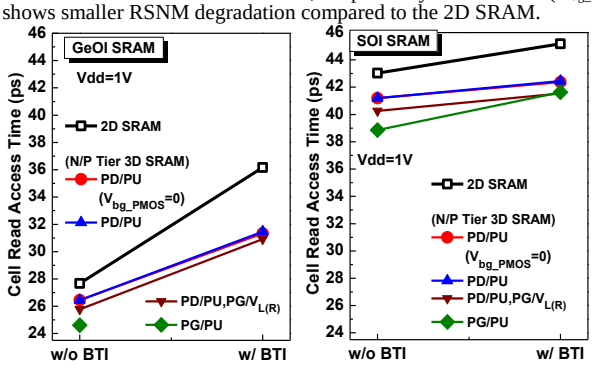

Fig. 10. Impact of BTI stress on the cell read-access time of 2D and various monolithic 3D GeOI and SOI SRAM cells, respectively. The PD/PU(V_{bg_PMOS}=0) shows smaller cell read access time degradation compared to the 2D SRAM.

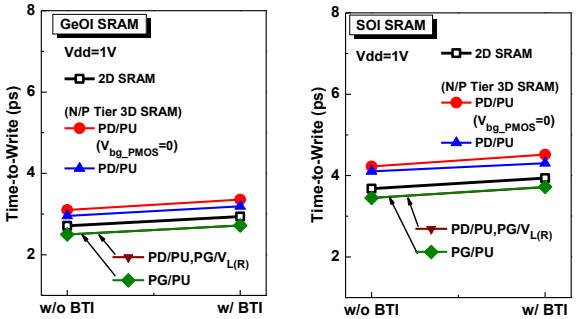

Fig. 11. Impact of BTI stress on the cell time-to-write of 2D and various monolithic 3D GeOI and SOI SRAM cells, respectively. The cell time-to-write degradations are comparable among 2D and 3D SRAM cells for both GeOI and SOI SRAMs