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A New NBTI Lifetime Prediction Method for Deeply Scaled pMOSFETs

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Abstract

RTN noise significantly affects the negative bias temperature (NBT) lifetime prediction for deeply scaled pMOSFETs. In this paper, a new difference method is proposed to reasonably separate the RTN noise component from the NBTI quasi static component of ΔV_{th}. The temperature and voltage accelerated factors of RTN noise intensity are extracted, showing good consistency with the tunneling process of RTN. A NBTI lifetime prediction model is further established at the accelerated NBT stress and the NBTI lifetime are predicted for small sized pMOSFETs.

1. Introduction

Random Telegraph Noise (RTN) is considered as a temporal variation caused by the capture and emission of channel carriers by defects inside the dielectric layer in CMOS devices [1-3]. It attracts much more attention recently as a dominant noise source in CMOS technology beyond the 45-nm node. Recent reports have revealed that RNT significantly affects the negative bias temperature instability (NBTI) in deeply scaled pMOSFETs, resulting in the poor accuracy and stability of NBTI lifetime prediction [4]. Some noise extraction methods have been proposed previously. The widely known one is the within-device-fluctuation (TVF) method, which separates the threshold voltage shift (ΔV_{th}) by NBTI quasi static component $\Delta V_{th,Min}$ and RTN fluctuation component $\Delta V_{th,Fluc}$ [4]. However, TVF method usually leads to the deviation of voltage and temperature characteristic of $\Delta V_{th,Fluc}$ from tunneling process of RTN noise[5].

In this paper, we propose a new difference method to characterize RTN noise component in NBTI lifetime data. This difference method takes advantage of picking up the relatively small noise signal from the time domain data. It can solve the problem of low detection accuracy yielded by the traditional method, and can avoid the heavily loaded computation caused by the algorithm of TVF method. The qualitative studies for RTN noise component of ΔV_{th} on the stress time, stress voltages and temperature are carried out. The NBTI lifetime prediction model with noise component is then constructed and the lifetime is predicted.

2. Experimental

pMOSFETs used in this study were fabricated with a standard 45 nm CMOS technology. The size of devices ($L \times W$) is 50 nm × 300 nm. The measurements were conducted using a Keithley 4200 semiconductor characterization system and a Cascade Summit 12000 probe station. Several device samples were measured under the same voltage and temperature condition to minimize the device-to-device variation using the Weibull distribution.

In the difference method, the threshold voltage shift $\Delta V_{th}(t)$ is considered to be consisted of two components:

$$\Delta V_{th}(t) = \Delta V_{th,average}(t) + \Delta V_{th,noise}(t) \qquad (1)$$

Here, $V_{th,average}$ is NBTI quasi static component and $\Delta V_{th,noise}$ is noise related component, here $\Delta V_{th,noise}$ (t) is obtained by calculating the ΔV_{th} difference value at t and $t + \Delta t$:

$$\Delta V_{th,noise}(t)=\Delta V_{th}(t+\Delta t)-\Delta V_{th}(t) \qquad (2)$$

$\Delta V_{th,average}$(t) is attained by extracting the average values in a time interval and then smoothly moving on the time trace to the next.

The detailed data processing steps for NBTI lifetime prediction are as follows: 1) Getting the time-dependent noise traces of $\Delta V_{th,noise}(t)$ in terms of Eq. (2); 2) Picking up a suitable time window (t-$\Delta t/2$ ~ t+$\Delta t/2$) on the time traces of $\Delta V_{th,noise}(t)$ to extract the noise standard variance which represents the intensity of $\Delta V_{th,noise}$ at t; 3) Using the smooth movement on the time traces of raw data ΔV_{th} to eliminate noise for $\Delta V_{th,average}$ extraction; 4) Measuring the voltage and temperature accelerated factors of $\Delta V_{th,average}$ and $\Delta V_{th,noise}$; 5) Predicting the NBTI lifetime under the operation condition based on the constructed NBTI lifetime prediction model.

3. Results and discussion

Fig. 1 shows the time dependence of threshold voltage shift ΔV_{th} under the NBT accelerated stress condition of V_{gs} = -1.9 V and T=125 °C. ΔV_{th} values represented by the symbol "o" in Fig. 1 are the simply average of several points per decade for lifetime prediction. Obviously, it does not capture the noise well. Moreover, when these values of ΔV_{th} from the discrete points taken from different devices are compared, the differences caused by the noise with time are mistaken as device-to-device variation.

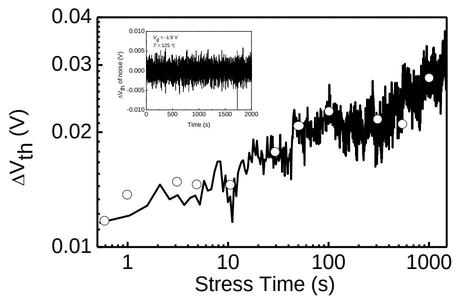

Fig. 1 Time traces of ΔV_{th} under the condition of V_{gs} = -1.9 V and T=125°C. The inset shows the extracted noise component based on the difference method.

The inset of Fig. 1 shows the extracted raw noise component based on the difference method. The component didn't exhibit the time dependence, informing that there is no new RTN traps generation. Fig. 2 presents the voltage and temperature dependence of the noise standard variance which represents the intensity of $\Delta V_{th,noise}$. It is seen that the higher the V_{gs} is, the greater the $\Delta V_{th,noise}$ is. The voltage accelerated factor is about 0.8; On the other hand, a negligible temperature dependence of $\Delta V_{th,noise}$ is observed, as shown in Fig. 2(b). The temperature and voltage behaviors of extracted noise intensity show good consistency with the physical properties of that of single RTN[6]. In the later case, a TAT model based on the hole tunneling via NBTI induced switching traps could explain the bias and temperature dependence of RTN amplitude in small size pMOSFETs.

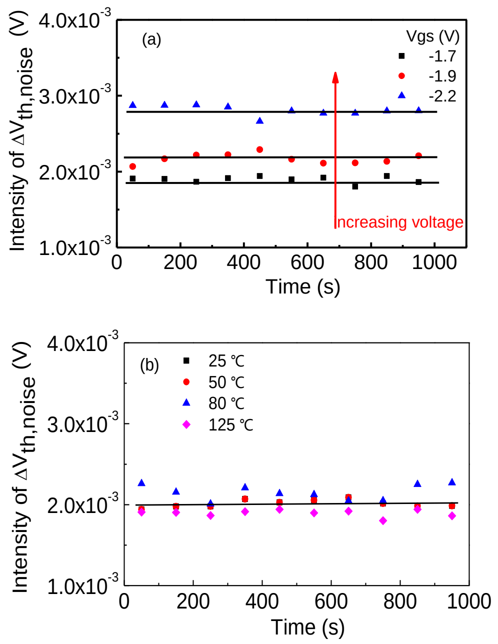

Fig. 2 Time dependence of $\Delta V_{th,noise}$ at various (a) voltage and (b) temperature stress.

Fig. 3 shows that the time dependence of $\Delta V_{th,average}$ obtained under the various voltage and temperature stress. It is clearly seen that the increase of the gate voltage and temperature lead to the degradation of $\Delta V_{th,average}$. A power time exponent of the $\Delta V_{th,average}$ is about 0.20. The obtained voltage and temperature accelerated factors of both $\Delta V_{th,average}$ and $\Delta V_{th,noise}$ are listed in Table I. According to these factors, we can predict NBTI lifetime for deeply scaled pMOSFETs by the following lifetime model:

$$\Delta V_{th} = \Delta V_{th,average} + \Delta V_{th,noise} = B*\exp(\beta_2 V_g)*\exp(-E_a / KT)*t^n + A*\exp(\beta_1 V_g) \quad (4)$$

The NBTI lifetime is estimated about 33 years at T=125 °C and V_{gs}=1.1*V_{dd}.

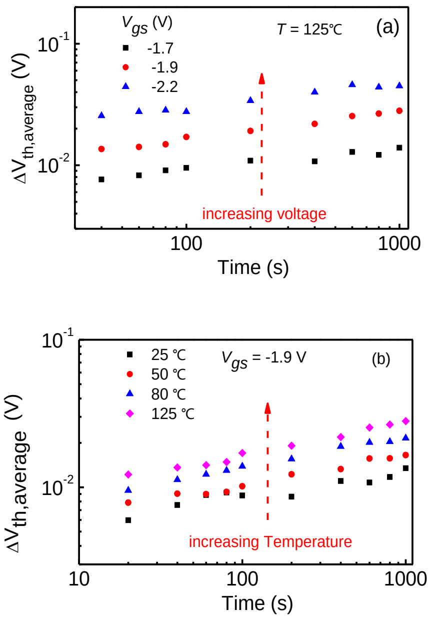

Fig. 3 Time dependence of $\Delta V_{th,average}$ under various (a) voltage and (b) temperature stress.

Table I. Temperature and voltage accelerate factors of $\Delta V_{th,average}$ and $\Delta V_{th,noise}$ components in NBTI degradation

Parameter	Difference Method	
	$\Delta V_{th,average}$	$\Delta V_{th,noise}$
n	0.20	0
β	2.0	0.8
E_a	0.08	0
Lifetime @ 125°C,V_{gs}=1.1*V_{dd}	33 years	

4. Conclusion

A new difference method is proposed to separate the noise related component from the NBTI quasi static component. The difference method not only reasonably extracts noise related component that shows good consistency with the physical properties of single RTN, but also successfully predicts the NBTI lifetime in deeply scaled pMOSFETs. It provides an accurate data processing method for noise analysis in scaled CMOS devices.

Acknowledgements

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