A-5-01(Invited)

Enabling Hetero-integration of III-V and Ge-based Transistors on Silicon with Ultra-thin Buffers formed by Interfacial Misfit Technique

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I. Introduction

III-V and Ge semiconductors have been researched as alternative channel materials for future technology nodes [1-28]. It is a challenge to integrate p- and n-FETs comprising different channel materials on Si substrates.

In this paper, we discuss the application of the interfacial misfit (IMF) technique to enable the heterogeneous integration of III-V and Ge-based transistors on Si substrates. IMFs are capable of relieving strain resulting from the large lattice mismatch between two materials and minimizing the formation of threading dislocations. In this work, Ge p-FETs and InAs n-FETs were co-integrated on a Si substrate using common contact formation, digital etch, and gate stack formation modules. In addition, vertically stacked GaSb nanowire p-FETs and InAs nanowire n-FETs on Si substrates were also realized with promising electrical characteristics.

II. GaSb Grown on GaAs using IMF Technique

The III-V layers in this work were grown using MBE on a GeOI (100) substrate with a 6° offcut. After the growth of a ~70 nm-thick GaAs buffer, a ~50 nm-thick GaSb layer was grown by employing the IMF technique. An array of misfits can be observed at the GaAs/GaSb interface as shown in the HRTEM image in Fig. 1 (a). These misfits relieve most of the strain in the 7.78 % lattice mismatched GaSb-GaAs system [15]. Under optimized growth conditions, the separation between two misfits is ~5.6 nm, implying that every 14th Ga atom from GaAs has a dangling bond [Fig. 1 (b)]. This confines the majority of the defects within a few nanometers at the GaAs/GaSb interface, so that subsequent layers with good quality can be grown for device fabrication.

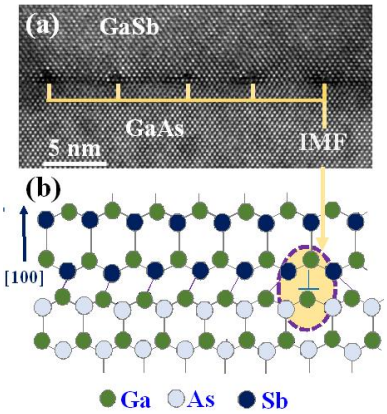

Fig. 1. (a) HRTEM image showing the periodic 2-D IMF array at the GaSb/GaAs interface. IMFs allow the relaxation of majority of the strain resulting from the lattice mismatch. (b) Schematic illustration of the misfits at the GaSb/GaAs interface.

III. Integration of Ge P-FETs and InAs N-FETs on a Si Platform

The first application of the engineered substrate is the monolithic integration of Ge p-FETs and InAs n-FETs using lift-off-free front-end process modules, as shown in the cross-sectional schematic of Fig. 2. Key features include: First, a sub-120 nm-thin III-V buffer growth technique was used to grow the good quality channel materials; Second, a common digital etch process was developed to precisely control the etch rates per cycle for n$^+$-InAs and Ge, enabling the formation of UTB structures; Third, Ge p-FETs and InAs

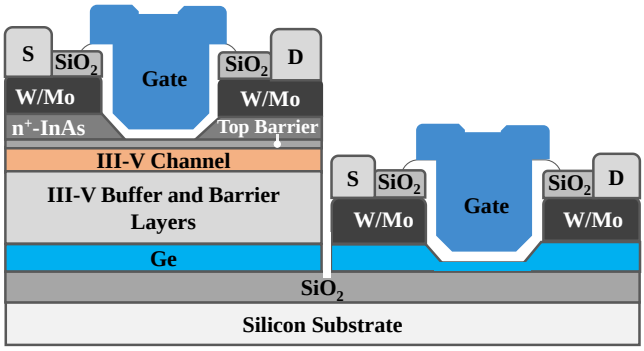

Fig. 2. Schematic of the first demonstration of InAs n-FETs and Ge p-FETs monolithically integrated on a Si substrate. The thickness of the III-V buffers is less than 120 nm.

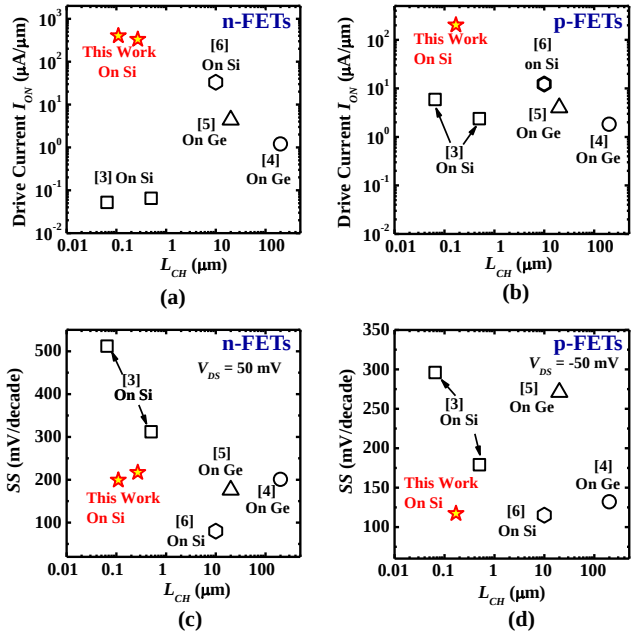

Fig. 3. (a) I_{ON} *vs.* L_{CH} *for* $In_{1-x}Ga_xAs$ n-FETs, (b) I_{ON} *vs.* L_{CH} *for* $Si_{1-x}Ge_x$ p-FETs [$|V_{GS}-V_{TH}|$=1 V and $|V_{DS}|$=1 V, except in [3] where $|V_{DS}|$=0.5 V], (c) *SS vs.* L_{CH} for $In_{1-x}Ga_xAs$ n-FETs, and (d) *SS vs.* L_{CH} for $Si_{1-x}Ge_x$ p-FETs. Note that the comparison is made among co-integrated SiGe p-FETs and InGaAs n-FETs on the Si substrate.

n-FETs share the same process modules to form the gate stacks and raised S/D structure.

Fig. 3 compares the drive current I_{ON} and subthreshold swing *SS* for monolithically integrated $Si_{1-x}Ge_x$ p-FETs and $In_{1-x}Ga_xAs$ n-FETs reported in literature with those realized in this work. Considering only co-integrated SiGe p-FETs and InGaAs n-FETs, I_{ON} achieved in this work is the highest at $|V_{GS}-V_{TH}| = |V_{DS}| = 1$ V (except in [3], $|V_{DS}| = 0.5$ V). *SS* for our Ge p-FETs is also comparable to the best value reported for Ge and SiGe p-FETs that are co-integrated with InGaAs n-FETs.

IV. Integration of GaSb P-FETs and InAs N-FETs based on Vertically-Stacked Nanowires on a Si Platform

Using III-V materials in the channels of both p- and n-FETs is another option for future low power and high performance logic applications. Here, we discuss the demonstration of monolithic integration of III-V p-FETs and n-FETs on a Si platform with vertically stacked III-V nanowires (Fig. 4). The InAs n-FETs and GaSb p-FETs were integrated on a common Si platform with multiple common process modules such as gate stack and contact processes. Promising device performance were achieved for both InAs n-FETs with a L_{CH} of 20 nm and GaSb p-FETs with a L_{CH} of 500 nm.

Fig. 5 compares I_{ON}/I_{OFF} ratio and *SS* of InAs n-FET and GaSb p-FET in this work with other reported in literature. Both I_{ON}/I_{OFF} ratio and *SS* were extracted at $|V_{DS}| = 0.5$ V. For InAs n-FETs, the devices realized in this work achieved the lowest *SS* and highest I_{ON}/I_{OFF} ratio for III-V CMOS on the Si substrate. For GaSb p-FETs, the I_{ON}/I_{OFF} and *SS* compare well with the best reported on III-V substrate and are much better than those of III-V CMOS on the Si substrate.

V. Conclusion

We demonstrated InAs n-FETs and Ge p-FETs integrated monolithically on Si substrate as well as the vertically stacked multi-gate InAs n-FETs and GaSb p-FETs integrated monolithically on the Si substrate. An important enablement is a novel IMF technique which achieves high quality channel layers using an extremely thin (sub-150 nm) III-V buffer. Good electrical characteristics were achieved for both n-FETs and p-FETs in the two integration schemes. This indicates that IMF technique is a promising approach to enable the integration of transistors employing Ge and III-V materials on a common Si platform.

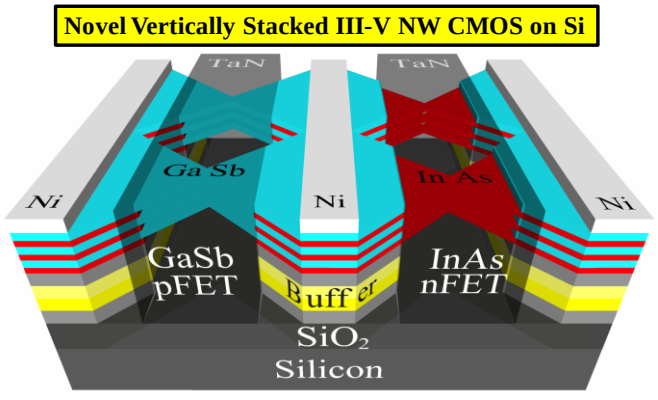

Fig. 4. 3D schematic of the vertically-stacked III-V nanowire CMOS on a common Si platform. This was enabled by growth of alternating layers of GaSb (p-FET channel) and InAs (n-FET channel) on a III-V buffer grown by IMF technique on a GeOI substrate (from Fig. 1 of Ref. 1).

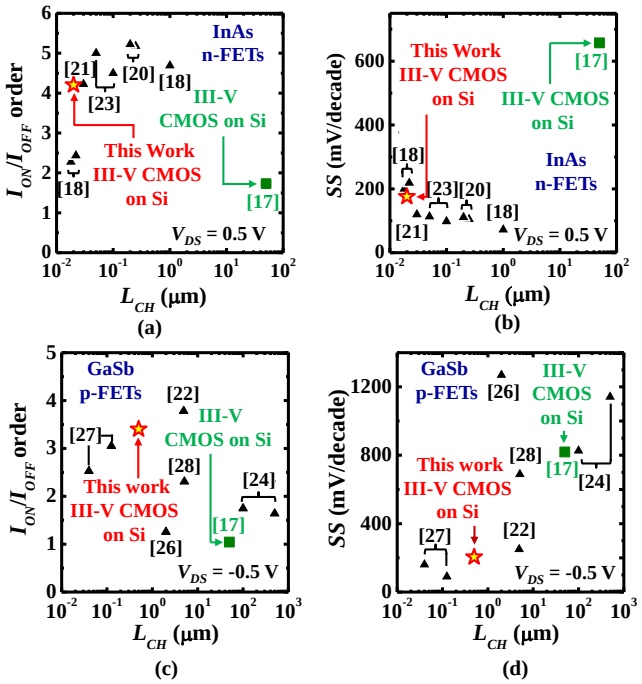

Fig. 5. Benchmark plot comparing (a) I_{ON}/I_{OFF} ratio of InAs n-FETs, (b) *SS* of InAs n-FETs, (c) I_{ON}/I_{OFF} ratio of GaSb p-FETs, and (d) *SS* of GaSb p-FETs. Our work achieved the best value of I_{ON}/I_{OFF} ratio and *SS* for III-V CMOS integrated on the Si substrate.

Acknowledgement. We acknowledge support from the Singapore National Research Foundation through a Competitive Research Program (Grant No: NRF-CRP6-2010-4).

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