A-5-04

On the Characterization of Hot Carrier Effect in Fully Depleted SOI and GeOI MOSFETs under Circuit-Speed Random Stress

Ran Cheng[1], Wenchao Chen[1], Da-Wei Wang[1], Jiwu Lu[3], Rui Zhang[1], Wen-Yan Yin[1], and Yi Zhao[1, 2*]

[1]College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China.
[2]State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou 310027, China.
[3]College of Electrical and Information Engineering, Hunan University,Changsha, 410082 China.
[*]E-mail: yizhao@zju.edu.cn

ABSTRACT

In this study, hot-carrier-injection (HCI) induced degradations under the circuit-speed random stress of FDSOI MOSFETs are investigated, for the first time. The circuit-speed random voltage stressed on the gate was mimicked by Pseudo Random Binary Sequence (PRBS) signals. It is found that the high frequency(>2 GHz) AC stress could introduce similar degradation as the PRBS stress, while the lower frequency AC and DC hot carrier injection (HCI) stresses induced higher degradations because of the self-heating effect. Therefore, to obtain a reliable HCI lifetime of FDSOI MOSFETs, a high frequency *f* (comparable with the circuit speed) AC HCI stress or a circuit-speed random stress is necessary. Furthermore, it is confirmed that GeOI device shows much severer self-heating issues than SOI device due to the larger I_{on} and lower thermal conductivity of Ge.

I. INTRODUCTION

To suppress short channel effects (SCEs), FinFETs are fabricated with more complicated process than planar devices [1]. An alternative way to suppress SCEs is to fabricate transistors on fully-depleted (FD) SOI substrates [2,3]. Recently, Ge MOSFETs fabricated on FD-GeOI substrates have been reported with excellent control of SCEs and decent on-state current [4]. However, with the insertion of buried oxide (BOX) layer, SOI MOSFETs suffer from severe self-heating effects (SHEs) due to the weak thermal coupling between the channel and the substrate. SHEs could not only cause device performance degradation but also introduce uncertainty in device reliability, especially for the high-density packed IC chips. In a working IC circuit, the current through the channel results in the localized heating, and the generated heat could affect the HCI behaviors. Therefore, in FDSOI MOSFETs, HCI is an eletro-thermal coupling process.

In "real" IC operation mode, the On and Off states of a transistor are random and unpredictable. Usually, the holding time of the On state is very short (<100 ps in the mainstream CPU). While in traditional simulations and experiments, the voltage wave is AC signals and the frequency is only at MHz level, which is significantly different from the case in real circuits.

In this work, we investigate the characterization of HCI under circuit-speed random stress for MOSFETs on FDSOI substrates, for the first time. PRBS, AC, and DC gate signals were applied to study the impact of SHEs on the device HCI lifetime. As Ge is one of the possible alternative channel material for sub-10 nm technology node, HCI lifetime with SHEs on FD GeOI MOSFETs were also provided.

II. CONCEPT AND MODENGING

A. The Impact of PRBS, AC and DC Signals

Fig. 1 illustrates the schematic of a Si MOSFETs with ultra-thin SOI and BOX layers. The transistors were covered with Si_3N_4 and the dimensions of the MOSFET were provided in Fig. 1. As shown in Fig. 1, the BOX layer would exempt the substrate leakage but introduce self-heating issues especially at the border of the channel and drain regions. The SHEs may cause the device performance degradation in terms of larger threshold voltage V_t, lower mobility and on-state current I_{ON} etc. Traditionally, HCI was characterized using DC or low-*f* AC signals (e.g.: 10 MHz or lower), resulting in the V_t degradation partially contributed from SHEs. While in the normal circuit operation mode, the gate signals were random and synchronized with the system clock. The heat generated in the channel region may be much less than that caused by DC and low *f* signals. However, as the real-time (GHz level) channel temperature *T* is not easy to be measured, it is difficult to experimentally separate the V_t shift due to HCI and that due to SHEs.

In this work, we modeled (Fig. 2) the heat characteristics of FDSOI MOSFETs with circuit speed PRBS, different frequency AC and DC signals (Fig. 3). Based on the transient channel temperature, we modeled the temperature-dependent electrical characteristics of the FDSOI transistors. V_t shift with different PRBS stress and other gate signal modes were compared and the effects on HCI characterization of these signals were investigated.

B. Electro-Thermal Modeling

Since the channel length of our SOI and GeOI transistors is in the scale of sub-100 nanometers, drift-diffusion equations (shown in Fig. 2) are applied to describe their carrier transport behavior. The simulated *I-V* characteristics is obtained by self consistently solving Poisson equation and current continuity equations [5]. Fig. 4 compares the fitted (symbols) and measured (lines) I_D-V_G characteristics of the FDSOI MOSFET (L_G = 100 nm, V_G = 1.2 V) in both linear and logarithm scales. The simulation results match well with the measure results. After that, the position dependent heat generation source can be calculated as $J \cdot E$. Time-dependent thermal conduction equation is solved with the update of temperature-dependent parameters for each time step.

III. DEVICE FABRICATION

Ultra-thin SOI wafers were used for FD Si MOSFET fabrication. The Si layer thickness is within 10 nm and the BOX layer thickness T_{BOX} is ~12 nm. Gate metal was sputtered, patterned and RIE etched with gate length L_G down to 100 nm. This was followed by n^+ S/D extension and SiN spacer formation. S/D implant and activation were performed followed by the epitaxially growth of raised S/D structure for lower S/D resistance. Ni silicide contacts were then formed. A layer of Si_3N_4 were deposited by CVD for better device isolation from contaminations and moistures. Contact holes were then opened for device characterization.

IV. RESULTS AND DISCUSSION

PRBS, AC (various frequencies) and DC signals were generated (Fig. 3) to compare the SHEs under PRBS, AC and DC signals. The zoomed-in details of the AC and PRBS signals were shown in Fig. 3(c) and (f), respectively. The rise and fall time (t_{rise} and t_{fall}, respectively) for the AC and PRBS signals are both 45 ps. The minimum time interval for V_G = 1.2 V in the PRBS is 90 ps and that for the AC signal is also 90 ps. Fig. 5 shows a transient temperature contour profile for the Si MOSFET with a PRBS gate signal. As expected, the channel/drain region exhibits the highest temperature *T* (~430 K). The resulting channel *T* (averaged over the channel) profiles were shown in Fig. 6. As compared with the DC signal (step pulse), both high-frequency (2.78 GHz) and PRBS gate signals shows much lower channel *T*. At *t* = ~200 ns, T_{DC}, T_{AC} and T_{PRBS} saturate and the values are ~580, 423, and 422 (Fig. 7), respectively. As V_t shift $\Delta V_T = V_{t0}(t/t_0)^n$, where n is proportional to *T* [6,7], we calculated ΔV_T for the three types of signals as a function of *t*, as shown in Fig. 8. Due to the severe SHEs, DC method shows much higher ΔV_T. The PRBS signal, which simulates the real circuit gate signal, exhibits much lower ΔV_T, suggesting that the DC method would underestimate the device lifetime. Furthermore, in most AC characterization process, the stress frequency is much lower (MHz level) than the one in Fig. 4(c). To investigate the effect of signal frequencies on ΔV_T, we simulated the channel temperature and calculated the corresponding ΔV_T as a function of *t*, as shown in Fig. 9 and 10, respectively. The channel *T* oscillates around a base *T*. As *f* decreases, the oscillation amplitude increases and the base *T* increases. A higher channel *T* leads to a higher ΔV_T. As we extended the trend line in Fig. 10 to 10 years, the difference between 2.78 GHz and 27.8 MHz increases by 50%. MOSFETs with thicker T_{BOX} was compared with the control in terms of ΔV_T under PRBS stress (Fig. 11). Due to the poor thermal conductance of BOX, devices with thicker T_{BOX} shows slightly higher channel *T*, and therefore higher ΔV_T. Fig. 12 shows the ΔV_T under various circuit speeds.

As Ge CMOS is one of the possible alternative for Si CMOS for sub-10 nm applications, we studied its HCI characteristics with SHEs (Fig. 13). When the channel changed from Ge to Si (Fig. 13 inset), the channel *T* increases from 432 K to 453 K (AC stress @ 278 MHz), and the 10 year ΔV_T is ~10% larger for the GeOI devices as compared to the SOI devices (Fig. 14).

Fig. 14 summaries ΔV_T in 10 years lifetime for various PRBS circuit speeds and AC stress signals. We could see that as the circuit speed increases, the ΔV_T is actually lowered.

V. CONCLUSION

We report the first modeling and characterization of HCI with SHEs on FDSOI MOSFETs under circuit-speed random stress or PRBS signals. The circuit-speed random stress and ultra-high *f* AC stress have similar effects on the HCI degradation of FDSOI MOSFETs. With the low-*f* AC and DC stress signals, the lifetime of SOI devices were underestimated, suggesting that under current or faster circuit-speed, SOI transistor exhibits less device degradation characteristics, making SOI structure a much promising candidates for ultra-scaled transistors. FD GeOI devices were also modeled. Further process development is necessary to mitigate the larger HCI degradation of GeOI MOSFETs as compared to the SOI transistors.

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Acknowledgement This work was supported by Natural Science Foundation of China (No. LR14F040001, No.61306097, No. 61376097 and No. 61431014).

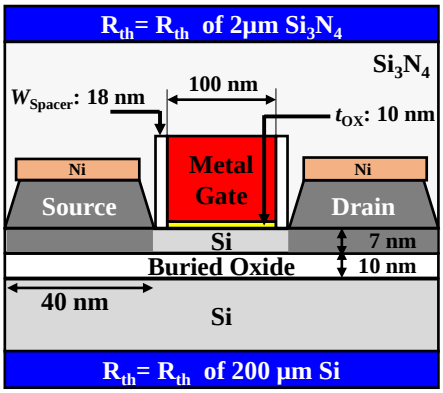
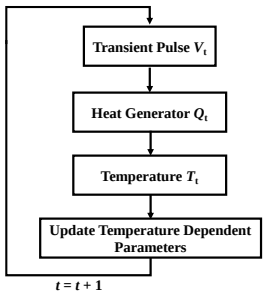


Fig. 1 Schematics of the SOI MOSFET for modeling and measurement. The dimensions used for simulation were indicated in the schematics. The Ni layer thickness is 20 nm, the raised S/D height is 11 nm and the gate height is 95 nm.



$$J_n = -qn\mu_n\nabla V + qD_n\nabla n$$
$$J_p = -qp\mu_p\nabla V - qD_p\nabla p$$
$$0 = \frac{1}{q}\nabla\cdot J_n + G_n - R$$
$$0 = -\frac{1}{q}\nabla\cdot J_p + G_p - R$$
$$-\nabla\cdot(\varepsilon_r\nabla V) = \frac{q}{\varepsilon_0}(p - n - N_A)$$

Fig. 2 Flow chart for transient thermal modeling. Electrical Modeling equaitions were also provided.

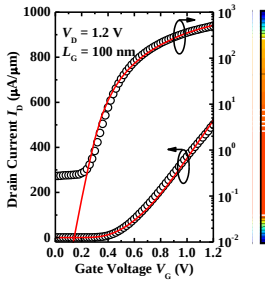


Fig. 4 I_D-V_G characteristics by simulation (solid) and by measurment (dot) match well.

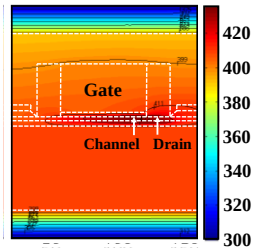


Fig. 5 Transient temperature profile in the device channel region shows the highest T of 430 K.

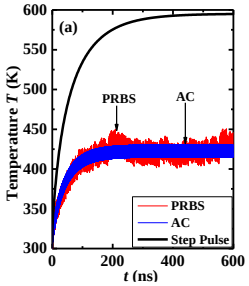


Fig. 6 Channel T-t plot shows high f AC and PRBS signal result much lower channel T than DC signal.

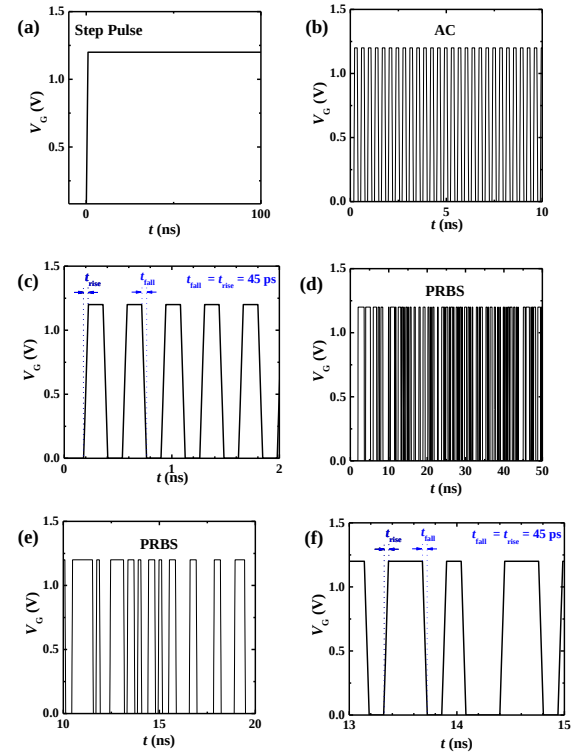


Fig. 3 (a), (b), (d) are the DC, AC and PRBS gate signals used for channel temperature and V_T shift calculation. The amplitude of the signals are 1.2 V. (c) is the zoomed-in AC signal within 2 ns. (e) and (f) are the zoomed-in PRBS signals with 10 and 2 ns, respectively. The rise and fall timefor the AC and PRBS signals are both 45 ps. The minimum time interval for V_G = 1.2 V in the PRBS is 90 ps and that for the AC signal is also 90 ps.

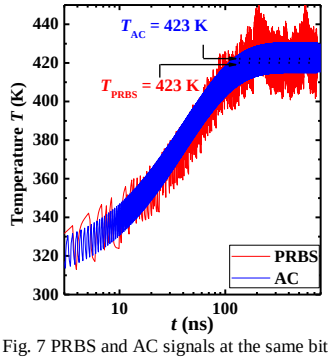


Fig. 7 PRBS and AC signals at the same bit rate show similar channel T profiles.

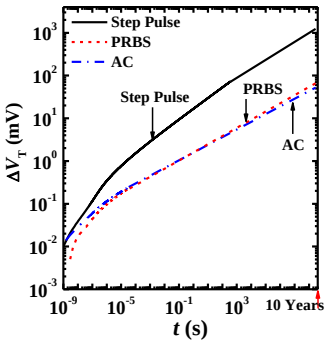


Fig. 8 ΔV_T-t plot are extended to 10 years. PRBS stress signal shows slightly higher ΔV_T.

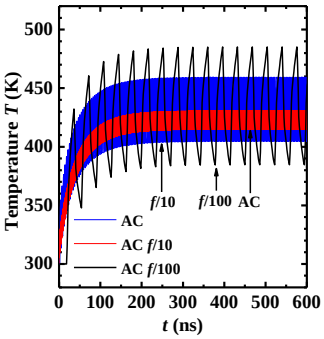


Fig. 9 Channel T-t plot shows higher f AC results in lower base channel T and smaller oscillation amplitude.

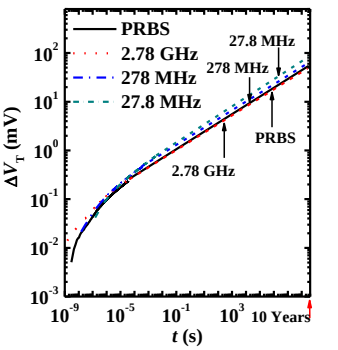


Fig. 10 ΔV_T-t plot are extended to 10 years for various f AC stress signal, lower f AC signals lead to much higher ΔV_T.

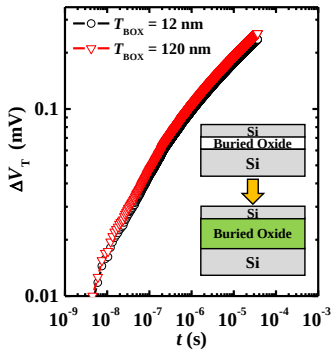


Fig. 11 Channel T-t plot shows devices with thinner BOX layer has lower base channel T The oscillation amplitude is comparable.

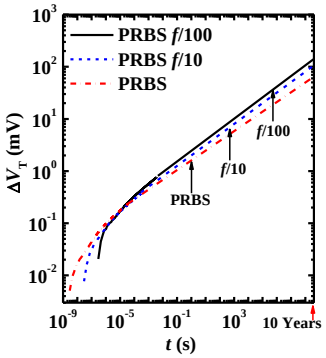


Fig.12 ΔV_T-t plot are extended to 10 years. for various f circuit speed, lower f PRBS signals lead to much higher ΔV_T

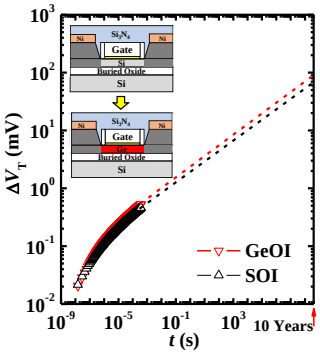


Fig. 13 ΔV_T-t plot are extended to 10 years for SOI and GeOI substrates.

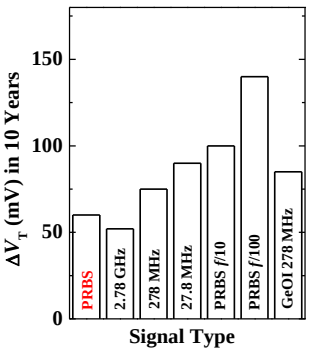


Fig. 14 Comparison ΔV_T for various signals and substrate types.