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Bias Temperature Instability in Tunnel FETs

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1. Introduction

The increasing power consumption of CMOS is a critical issue. Tunnel FETs (TFETs), which can realize a steep subthreshold slope (SS) of less than 60 mV/dec, are promising ultralow-power devices [1-3]. Since TFETs are assumed to have ultralow-voltage operation, the BTI criteria of TFETs are more severe than those of MOSFETs. It is important to clarify the BTI mechanism to achieve TFETs with the long-term reliability. Recently, many studies on the PBTI of n-type TFETs have been reported [4-6]; however, the detailed BTI mechanism, including NBTI, in TFETs has not yet been understood.

There are two main differences between TFETs and MOSFETs (Fig. 1). One is the operation mechanism and the other is the polarity of the source/drain (S/D). TFETs operate by band-to-band tunneling, whereas MOSFETs operate by drift and diffusion. The polarity of the S/D in TFETs is asymmetric, while it is symmetric in MOSFETs. These differences are important in understanding the BTI mechanism of TFETs.

In this paper, we investigated the BTI mechanism of TFETs from three viewpoints as shown in Fig. 2.

2. Experimental Method

N-type TFETs (nTFETs) with a (110) fin channel and p-type TFETs (pTFETs) with a (100) planar channel were fabricated on (100) SOI substrates. N^+ poly-Si/$HfAlO_x$/SiO_2 (equivalent oxide thickness (EOT) = 2.2 and 2.4 nm) gate stacks were formed for the nTFETs and n^+ poly-Si/TaN/HfO_2/SiN (EOT = 0.74 and 0.85 nm [1]) gate stacks were formed for the pTFETs. Subsequently, the gate electrode was formed by EB lithography and dry etching. In the nTFET, BF_2^+ was implanted at 5 keV with a dose of 1.0×10^{15} cm^{-2} in the source region and As^+ was implanted at 5 keV with a dose of 1.0×10^{15} cm^{-2} in the drain region [7]. In the case of the pTFET, an n^+ source was formed by As^+ implantation and a p^+ drain was formed by BF_2^+ implantation [1]. Flash lamp annealing was performed at 1200 °C for 3 ms for the n- and p-type TFETs. The back-end process was carried out.

3. Results and Discussion

3.1. PBTI in N-type Tunnel FET

In the nTFET (Fig. 3), V_{th} shifts in the positive direction under positive bias stress, regardless of the stress voltage (Fig. 4). ΔV_{th} follows a power-law of stress time and the exponent n is about 0.1 (Fig. 4). On the other hand, SS is not degraded by PBTI degradation (Fig. 5). The activation energies causing PBTI degradation are 0.026 eV for the nTFET and 0.022 eV for the nFET (Fig. 6), which means that the PBTI mechanism of the nTFET is the same as that of the nFET. The PBTI degradation of the TFET is mainly caused by the electron traps generated in high-k films. On the other hand, the interface state is not degraded by PBTI. This is consistent with no SS degradation in Fig. 5.

In the case of the TFET, the polarity of the S/D is asymmetric (Fig. 2). Next, we investigated the impact of each carrier injection from the S/D on PBTI degradation. Figure 7 shows ΔV_{th} at 1000 s as a function of the applied voltage - V_{th} in the nTFET under various stress conditions. The gate/p^+ source stress corresponds to electron injection from the n^+ drain, while the gate/n^+ drain stress corresponds to tunneling carrier injection from the p^+ source. ΔV_{th} at 1000 s for the gate/p^+ source stress is almost the same as that for the conventional gate stress. In contrast, the value of ΔV_{th} at 1000 s for the gate/n^+ drain stress is very small. Thus, these results indicate that the PBTI degradation of the nTFET is mainly caused by electron injection from the n^+ drain.

3.2. NBTI in P-type Tunnel FET

Figure 9 shows $-\Delta V_{th}$ as a function of stress time under negative bias stress for the pTFET (Fig. 8) of sub 60 mV/dec. V_{th} shifts in the negative direction under negative bias stress. The SS increases with the stress time regardless of the stress E_{eff} (Fig. 10), which means that the SS is degraded by NBTI degradation. The activation energies causing NBTI in the pTFET and pFET are almost the same (Fig. 11). This means that the NBTI mechanism of the pTFET is the same as that of the pFET. Thus, holes are mainly trapped in high-k films by negative bias stress in the pTFET and also the interface state is degraded.

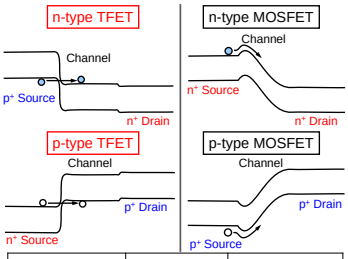
From the separate evaluation of each type of carrier injection from the S/D, it was found that the NBTI of the pTFET is caused by tunneling carriers injected from the n^+ source and holes injected from the p^+ drain (Fig. 12). In the case of the TFET, BTBT occurs in the local region near the source/gate edge (Fig. 2). Next, we studied the impact of traps and interface state degradation locating the BTBT region or the non-BTBT region in the gate dielectrics on NBTI degradation by simulation. Figure 13(b) shows the $-I_d$–V_g characteristics before and after NBTI for the pTFET. In the case that traps and interface state degradation are located in the BTBT region (Fig. 13(a)), the simulation data are well fitted to the measured result after NBTI degradation. On the other hand, in the case of the non-BTBT region (Fig. 13(a)), the simulated $-I_d$–V_g characteristics well reproduce the measured result of the initial state. Thus, the negative V_{th} shift due to NBTI in the pTFET is mainly caused by traps and interface state degradation located in the BTBT region. Traps and interface state degradation in the non-BTBT region have little impact on the V_{th} shift caused by NBTI degradation.

4. Conclusion

We investigated the BTI mechanism of TFETs (Fig. 14). Each BTI mechanism of n- and p-type TFETs is the same as that of MOSFETs. Although the injection sources of carriers causing BTI degradation in TFETs are different for PBTI and NBTI, BTI in TFETs is caused by traps and/or interface state degradation located in the BTBT region near the source/gate edge.

Acknowledgements This work was supported in part by NEDO and by JSPS through First Program initiated by CSTP.

References [1] T. Mori et al., Appl. Phys. Express **7** (2014) 024201. [2] Y. Morita et al., Symp. on VLSI Tech. Dig. (2013) T236. [3] T. Mori et al., Symp. on VLSI Tech. Dig. (2014) 86. [4] G. F. Jiao et al., IEDM Tech. Dig., (2009) 741. [5] W. Mizubayashi et al., IEDM Tech. Dig. (2014) 824. [6] A. Alian et al., IEDM Tech. Dig. (2015) 823. [7] T.Mori et al., JJAP **50** (2011) 06GF14-1.[8] HyENEXSS, ver. 5.5. [9] K. Fukuda et al., Proc. SISPAD (2012) 284.



	TFET	MOSFET
Operation Mechanism	BTBT	Diffusion and Drift
Polarity of S/D	Asymmetry	Symmetry

Fig. 1. Schematic illustration of main differences between TFETs and MOSFETs.

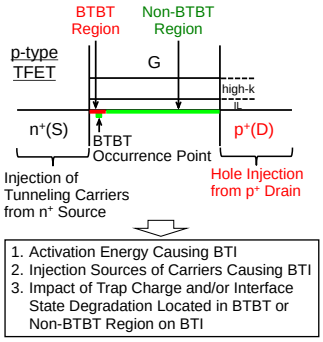


Fig. 2. Schematic illustration of investigation of BTI degradation in TFET.

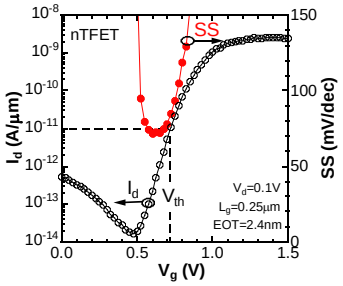


Fig. 3. I_d and SS–V_g characteristics of nTFET with EOT = 2.4 nm. V_{th} was defined as the gate voltage (V_g) at a drain current ($|I_d|$) of 10^{-11} A/μm.

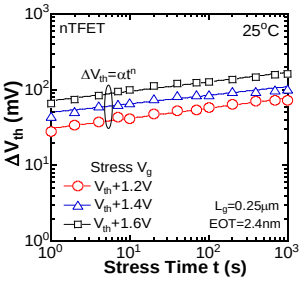


Fig. 4. ΔV_{th} as a function of stress time in nTFET.

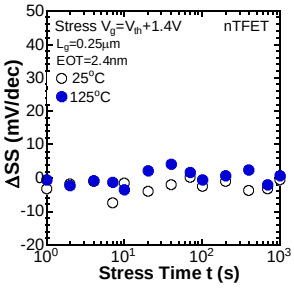


Fig. 5. ΔSS as a function of stress time for nTFET. SS was defined as $|dV_g/dlog_{10}|I_d||$ in the range from $|I_d|$ = 10^{-12} to 10^{-11} A/μm.

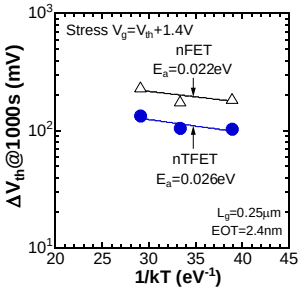


Fig. 6. Arrhenius plots of ΔV_{th} at 1000 s at stress V_g = V_{th}+1.4V for nTFET and nFET.

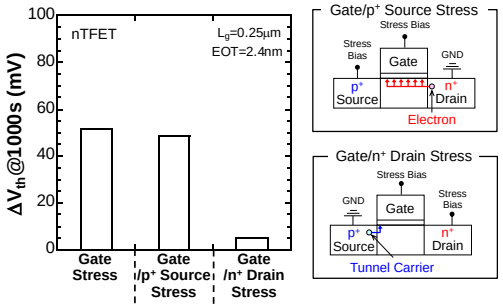


Fig. 7. ΔV_{th} at 1000 s for nTFET under various stress conditions.

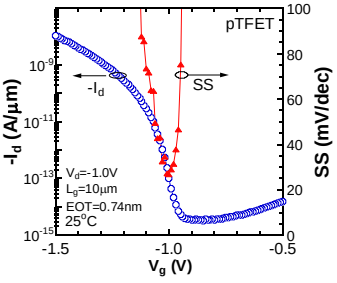


Fig. 8. -I_d and SS–V_g characteristics for pTFET [1] with EOT = 0.74 nm.

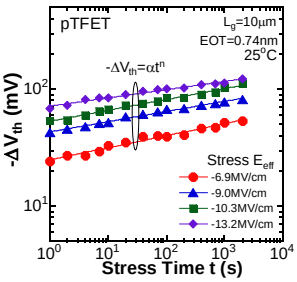


Fig. 9. -ΔV_{th} as a function of stress time under negative bias stress for pTFET with EOT = 0.74 nm.

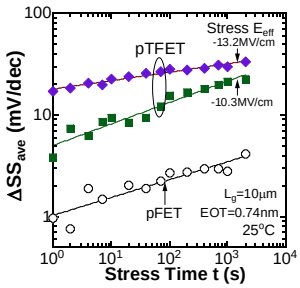


Fig. 10. ΔSS_{ave} as a function of stress time under negative bias stress for pTFET with EOT = 0.74 nm.

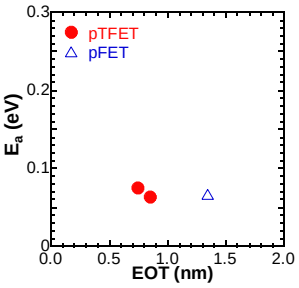


Fig. 11. Activation energy (E_a) of ΔV_{th} caused by NBTI degradation as a function of EOT for pTFET.

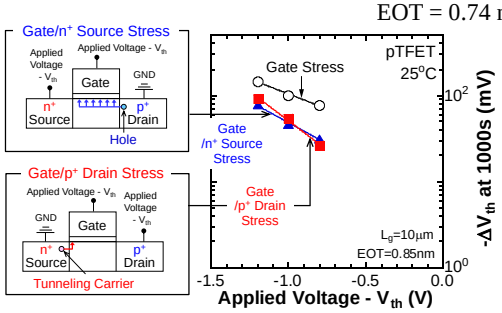


Fig. 12. ΔV_{th} at 1000 s as a function of applied voltage -V_{th} for pTFET under various stress conditions.

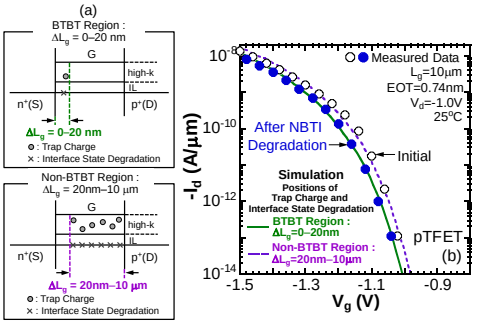


Fig. 13. (a) Schematic illustration of cross section of gate dielectrics after NBTI degradation. (b) I_d–V_g characteristics for pTFET. The simulation was performed using HyENEXSS ver. 5.5 [8, 9].

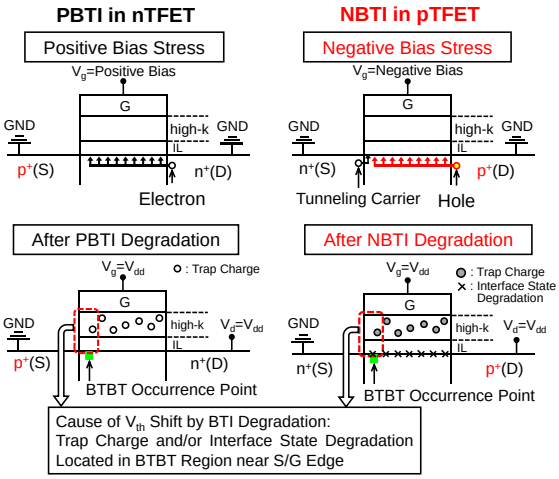


Fig. 14. Schematic illustration of BTI degradation for n- and p-type TFETs.